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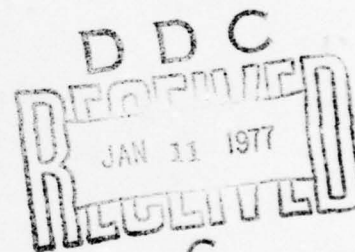
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AN EVALUATION OF CHARGED-COUPLED DEVICES TECHNOLOGY

R. L. Anderson
Department of Defense
U. S. Air Force
Rome Air Development Center
Rome, N.Y. 13441



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<p>16. Abstract</p> <p>The principles of operation of charged-coupled devices (CCD's) are presented and the variety of structural forms currently used are described along with processing methods.</p> <p>The capabilities and limitations of CCD's and their input and output circuits are discussed. The uses of CCD's as digital circuits, as analog circuits and as image sensors are outlined. The report concludes with an overall evaluation of CCD technology.</p>			
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LENGTH

in	inches	*2.5	cm	centimeters
ft	feet	30	m	meters
yd	yards	0.9	m	meters
mi	miles	1.6	km	kilometers

AREA

in ²	square inches	6.5	cm ²	square centimeters
ft ²	square feet	0.09	m ²	square meters
yd ²	square yards	0.8	m ²	square meters
mi ²	square miles	2.6	km ²	square kilometers
	acres	0.4	ha	hectares

MASS (weight)

oz	ounces	28	g	grams
lb	pounds	0.45	kg	kilograms
	short tons (2000 lb)	0.9	t	tonnes

VOLUME

tsp	teaspoons	5	ml	milliliters
fl oz	fluid ounces	15	ml	milliliters
c	cups	30	l	liters
pt	pints	0.24	l	liters
qt	quarts	0.47	l	liters
gal	gallons	0.95	l	liters
ft ³	cubic feet	3.8	m ³	cubic meters
yd ³	cubic yards	0.03	m ³	cubic meters
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TEMPERATURE (exact)

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FOREWORD

This report was prepared for the Federal Aviation Administration (FAA) under the Post-Doctoral Program of the Rome Air Development Center (RADC) via the Reliability and Compatibility branch of RADC. The responsible persons are Mr. Fred Sakete at the FAA, Mr. Ed O'Connell at RADC, and Mr. Jacob Scherer of the Post-Doctoral Program. Dr. Henry Domingos of Clarkson College of Technology is the group leader for evaluation of a series of integrated circuit technologies under this program, including silicon on sapphire (SOS), Emitter Coupled Logic (ECL), Integrated Injection Logic (I^2L), and Charge-Coupled Devices (CCD's).

The RADC Post-Doctoral Program is a cooperative venture between RADC and some sixty-five universities eligible to participate in the program. Syracuse University (Department of Electrical and Computer Engineering), Purdue University (School of Electrical Engineering), Georgia Institute of Technology (School of Electrical Engineering), and State University of New York at Buffalo (Department of Electrical Engineering) act as prime contractor schools with other schools participating via sub-contracts with the prime schools. The U.S. Air Force Academy (Department of Electrical Engineering), Air Force Institute of Technology (Department of Electrical Engineering), and the Naval Post Graduate School (Department of Electrical Engineering) also participate in the program.

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Further information about the RADC Post-Doctoral Program can be obtained from Jacob Scherer, RADC, tel. AV 587-2543, COMM (315) -330-2543.

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1. INTRODUCTION

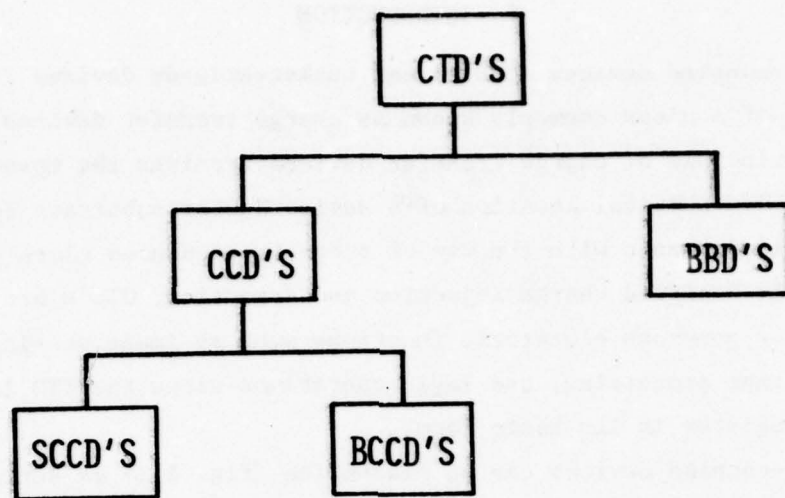
Charge-coupled devices (CCD's) and bucket-brigade devices (BBD's) are subsets of a class commonly known as charge transfer devices (CTD's). The basic principle of charge transfer devices involves the movement of charge from one physical location of a semiconductor substrate to another in a controlled manner with the use of properly sequenced clock pulses. With properly designed charge injection and detection, CTD's are capable of performing numerous electronic functions such as image sensing, data storage, signal processing, and logic operations since the CTD is an analog shift register in its basic form.

Charge-coupled devices can be classified (Fig. 1.1) as surface charge-coupled devices (SCCD's) in which the signal charge is transferred along the Si surface (or, more accurately, the Si/SiO₂ interface), or bulk charge-coupled devices (BCCD's) in which the signal charge is transported within the Si.

1.1. History and Development of CCD's

The concept of storing information via charge in a capacitor is not new. The concept of connecting a series of storage capacitors with perfect switches was adapted to provide a variable analog delay line. However, the charge transfer concept lacked an effective vehicle to develop and utilize these ideas. With the recent significant process and material improvements associated with MOS technology, and control of Si/SiO₂ interface properties, it became possible to translate these ideas into physically realizable devices. The first modern implementations of the charge transfer concept employed bipolar transistors as switches (1,2). The bipolar transistors were later replaced by MOS transistors (3,4) and the form now known as bucket-brigade devices was developed (4).

The CCD concept was initially developed in 1969 by Boyle and Smith (6) and was later verified in 1970 (5). According to this concept, the switches between the storage capacitors were removed by placement of adjacent capaci-



- CTD'S - CHARGE TRANSFER DEVICES
- BBD'S - BUCKET BRIGADE DEVICES
- CCD'S - CHARGE-COUPLED DEVICES
- SCCD'S - SURFACE CHARGE-COUPLED DEVICES
- BCCD'S - BULK CHARGE COUPLED DEVICES

Figure 1.1. Family of Charge Transfer Devices

tors in close proximity of each other. The stored charge is maintained in the surface layer of silicon in inversion regions, which are induced by electrodes located on top of a thin (100nm) silicon dioxide layer. By a proper sequence of voltage pulses on adjacent electrodes, the inversion region under the first electrode can be made to collapse as the next inversion region expands. Thus the potential well and its associated minority signal charge is effectively passed on to the next electrode. A 3-phase p-channel CCD (6) was investigated theoretically following the initial concept but the first CCD circuit actually incorporating these concepts was an 8-bit shift register (7). To increase the efficiency of charge transfer and to decrease the required number of clocks, differing forms of CCD's were independently devised. Placing a transfer electrode between, and overlapping, the two storage electrodes reduced the effective signal charge loss during charge transfer (8). Numerous contributors have since attempted to devise improved structures from the basic CCD concept.

From the initial simple 8-bit shift register, the first major application of the CCD technology was in signal processing because these devices can provide accurate, clock-controlled time delays of analog signals. Signal processing circuits such as analog delay lines, multipliers, recursive filters, transversal filters, correlators, etc. have been developed which utilize the analog delay effects. It was later realized that image sensors could also be constructed by generating the minority signal charge by optical means. Both linear and area image sensors have been developed which are capable of detecting visible light. With slight modifications, the image sensor concept was extended to the infrared spectrum. The CCD concept was further adapted to generate large digital memory arrays for medium speed, mass storage applications.

1.2. Characteristics and Advantages of CCD's

The main feature of CCD technology is its capability to provide accurate, clock-controlled time delays of analog signals. Although bucket-brigade devices can also perform this function, almost all CCD structures have

inherently better performance than equivalent bucket-brigade devices, especially in the areas of charge transfer efficiency and transfer noise. Thus, even though bucket-brigade devices were developed before CCD's, the CCD technology now dominates (except in very specific applications), and bucket-brigade device utilization has been rendered insignificant in comparison to CCD usage.

As initially conceived, the CCD theory was relatively simple and therefore fabrication was simple as compared to standard MOS technology. However, as the concept matured, the CCD structure and fabrication process evolved until now CCD processing is appreciably more involved than silicon-gate MOS processing. Multiple silicon gate levels, diffused or implant channel confinement structures, implanted barriers, etc. are now commonly utilized in addition to standard silicon-gate MOS processing. CCD processing does allow the usage of MOS circuits on the same chip for clock, input, detection, etc. circuits. However, the simplicity of the basic cell structure still remains and thus the circuit packing density of a CCD is significantly higher than silicon-gate MOS circuits. Processing is also simplified and yields are improved by the elimination of intercell connections. CCD circuits offer low noise and low power advantages where the power requirements are approximately 1-5 $\mu\text{W/bit}$ at 1MHz. CCD circuits are in the medium speed range with data shift rates normally about 5-20 MHz with some special designs at 135 MHz. However, CCD operation is dynamic in nature since thermal generation of carriers will in time oblivate the signal charge.

CCD image sensors have excellent low light level response, and cooled CCD imagers are capable of detecting a very small number of photons. Ability to detect 1 photon has been predicted. Because of the high packing density, the number of sensors per unit area is quite high, typically one site per square mil. CCD imagers integrate the charge which is generated by the incoming light by collecting charge for a certain time and then reading it out. This accounts for its favorable low light level response. In signal processing applications, CCD's use their variable input signal charge and

variable time delay to perform analog functions which are difficult if not impossible to implement economically in other technologies. Transversal and recursive filters have been manufactured which can have electronically variable bandwidth and center frequency, leading to spread spectrum communication applications. Using the non-destructive data sampling which is possible with CCD's, multiplexers, as well as other circuits such as correlators, shift registers, etc. are simple to construct.

A more recent application of CCD's is in the area of large memory arrays. CCD memories, organized in line or track form, consist of circulating serial shift registers. Address circuitry is located on the chip, and addresses each track which is then read out serially. Most line lengths are 64 or 128 bits long, and average access time for any bit is approximately 50 μ s for a 128 bit line. High packing density is of extreme importance, and currently 16K CCD memories are available in a single reasonably sized chip. CCD memories, which are volatile, need regenerative circuitry on chip to maintain the data. Main competition for CCD memories come from magnetic bubble memories and disc memories. Disc memories, while currently firmly established in this memory area, are slower and less reliable than CCD memories. Furthermore, they have extensive overhead equipment requirements which make the system physically large and of high power consumption. Magnetic bubbles have low power, data nonvolatility, non-diffusion or implant processing, and no standby power requirements which are advantages as compared to CCD's. However, magnetic bubble memories require high cost, complex materials, high performance sense amplifiers, and off-chip input and detection circuitry, as well as having slower speed capabilities than CCD's.

1.3. Scope of this Report

This report attempts to cover in some detail the current state-of-the-art of charge-coupled device technology. It is obvious from the number of references involving CCD's that the field has developed rapidly since its inception approximately six years ago, and a complete survey is therefore difficult to achieve accurately. It should be noted that an excellent book (9)

of charge transfer device technology has recently been published and complements this report in many areas.

This report is divided into three general sections. The first part, consisting of chapters 2 and 3, describes the fundamental theory concerning CCD technology and illustrates the variety of structural forms which are currently used. The methods of injecting and detecting the minority signal charge are discussed as well as the processing techniques of CCD's with MOS device processing used as reference. The capabilities and limitations of CCD's are presented, and areas such as signal handling, transfer inefficiency, noise and dark currents, and power are evaluated. The following section, chapter 4, deals with the current utilization of the CCD concept and investigates digital circuits, analog circuits, image sensors, and their performance characteristics. In the third section, chapters 5 and 6, the important areas of basic device costs, reliability, industrial trends, and recommendations are offered to indicate where CCD's are currently used and where the CCD technology can be used in the future.

Schematic diagrams are used extensively in this report to indicate the various physical structures of CCD's. To avoid confusion, the code indicated in Fig. 1.2 is used throughout in hybrid schematic diagrams*. Diagrams representing the topography or surface view do not use this code.

* By hybrid we refer to a schematic of the structured cross-section on a plane perpendicular to the surface. Superimposed on this are potential wells for free electrons. The depth of the well indicates the minimum potential energy in the Si.

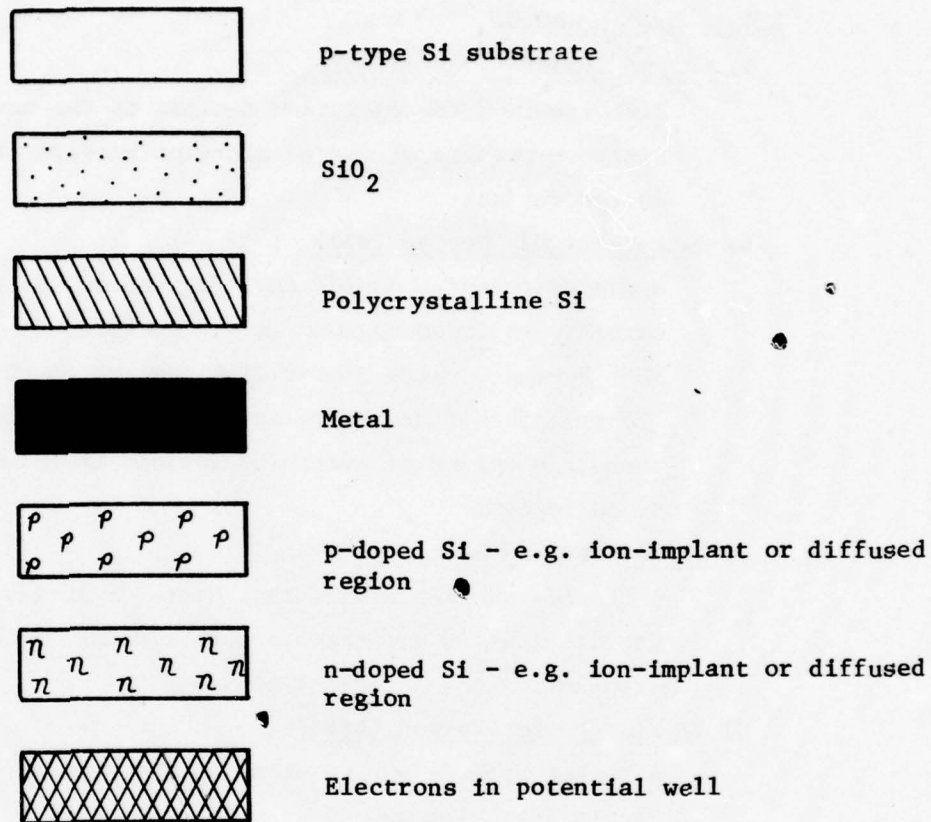


Figure 1.2. Code for hybrid diagrams

1.4. Definition of Terms

The following are typical definitions related to charge-transfer devices which are currently in use.

1.4.1. Device names.

a) Charge-Transfer Device (CTD).

A device in which operation depends on the movement of discrete packets of charge along or beneath the semiconductor surface.

b) Bucket-Brigade Device (BBD).

A charge-transfer device that (1) stores charge as majority carriers in doped regions in the surface of a semiconductor that become reverse biased with respect to the substrate and (2) transfers this charge as a packet along the surface through a series of switching devices that interconnect the doped regions.

c) Charge-Coupled Device (CCD).

A charge-transfer device that stores minority carriers in potential wells and transfers this charge as a packet by translating the potential minima.

d) Bipolar Bucket-Brigade Device.

A bucket-brigade device in which the switching devices are bipolar transistors.

e) JFET Bucket-Brigade Device (JFET BBD).

A bucket-brigade device in which the switching devices are junction-gate field-effect transistors.

f) MOS Bucket-Brigade Device (MOS BBD).

A bucket-brigade device in which the switching devices are MOS field-effect transistors.

g) Surface-Channel Charge-Coupled Device (SCCD).

A charge-coupled device in which the potential wells are created at the semiconductor-insulator interface and charge is transferred along that interface.

h) Buried-Channel Charge-Coupled Device (BCCD).

A charge-coupled device that confines the flow of charges to a channel lying beneath the surface.

i) Bulk-Channel Charge-Coupled Device (BCCD).

A synonym for buried-channel charge-coupled device.,

j) Conductively-Connected Charge-Coupled Device (C4D).

A charge-coupled device that uses doped regions between the potential wells and hence becomes a hybrid between a charge-coupled device and a bucket-brigade device.

k) Junction-Gate Charge-Coupled Device.

A buried-channel charge-coupled device that uses a diffused junction as the gate electrode.

l) Schottky-Barrier Charge-Coupled Device.

A buried-channel charge-coupled device that uses a Schottky barrier junction as the gate electrode.

m) Charge-Coupled Image Sensor.

A charge-coupled device in which an optical image is converted into packets of charge that can be transferred as the electrical analog of the image.

n) N-Channel Charge-Coupled Device.

A charge-coupled device fabricated so that the charges stored in the potential wells are electrons.

o) P-Channel Charge-Coupled Device.

A charge-coupled device fabricated that the charges stored in the potential wells are holes.

p) Multiphase Charge-Coupled Device.

A charge-coupled device that requires more than one clock applied sequentially to provide directionality to the transfer of charge.

q) Uniphase Charge-Coupled Device; One-Phase Charge-Coupled Device.

A charge-coupled device that has asymmetric potential wells so that only a single clock is necessary to transfer the charge in the desired direction.

r) Overlapping Gate Charge-Coupled Device.

A charge-coupled device formed so that adjacent gate electrodes overlap and are insulated from one another.

1.4.2. General Terms.

a) Background Charge.

Synonym for circulating bias charge used mainly in imaging devices.

b) Charge Packet.

A quantity of electrical charge that is the sum of the signal charge and bias charge (if used) and is stored in potential wells.

c) Charge-Regeneration Stage.

A region of a charge-transfer device that is used to refresh digital information stored in a bit location.

d) Circulating Bias Charge.

A quantity of electrical charge that is inserted into the potential well to define the low charge level.

e) Drift-Aiding Fringing Field.

An electric field at the semiconductor-insulator interface along the direction of charge propagation due to the potential on adjacent gate electrodes and the potential on the gate electrode directly above.

f) Empty Zero.

A condition where there is zero circulating bias charge.

g) Fat Zero.

Synonym for circulating bias charge and used mainly in digital devices.

h) Floating Diffusion.

A diffused area into which a charge packet can be introduced thereby changing its potential.

Note: Typically used in detection or regeneration schemes.

i) Floating Gate.

An electrically floating gate (pad) on an insulating surface over an active portion of the semiconductor surface.

Note: Typically used in detection or regeneration schemes.

j) Gate Electrode; Transfer Electrode.

A plate (pad) that is on an insulating surface over an active portion of the semiconductor surface and to which potential is applied.

k) Potential Minimum.

A local minimum of the electrostatic field.

l) Potential Well.

A spatially defined depletion region of a charge-coupled device where a potential minimum exists.

m) Signal Charge.

A quantity of electrical charge in a potential well that, in conjunction with the bias charge (if used), defines the signal level.

n) Skinny Zero.

Synonym for circulating bias charge of smaller magnitude than for Fat Zero (normally applied to BCCD's).

o) Transfer Channel.

The area of a charge-coupled device in which the charge flow is confined.

Note: This is physically accomplished by means of an oxide step, a channel-stopping diffusion or implant, or by a special edge-guard electrode.

p) Stage

That part of a CCD which forms the smallest definable operation. It consists of one storage gate and accessory transfer gates, if used.

q) Element

The smallest portion in a CCD delay line which upon translation can generate the complete line. In a p-phase system each element contains p stages.

r) Unit Cell

Synonym for element.

1.5 Notation

A	Area
A_B	Area occupied by background charge
A_S	Area occupied by signal packet
A_{St}	Area of storage electrode
A_k	Feedback coefficient
B	Bandwidth
b_k	Feedback coefficient
C	Capacitance per unit area
C'	Capacitance
$C'_D (C_D)$	Capacitance (capacitance per unit area) of depletion region
$C'_{eff} (C_{eff})$	Effective capacitance (capacitance per unit area) of channel
$C'_{FD} (C_{FD})$	Capacitance (capacitance per unit area) of floating diffusion
$C'_{FG} (C_{FG})$	Capacitance (capacitance per unit area) of floating gate
C_{GB}	Capacitance per unit area between gate and substrate
C_M	Capacitance per unit area of metering well
C_{ox}	Capacitance per unit area associated with oxide

C_{ox}^{st}	Oxide capacitance per unit area of storage electrode
C_{ox}^{tr}	Oxide capacitance per unit area of transfer electrode
C'_s	Capacitance of source
D	Diffusion Coefficient
D_n	Diffusion Coefficient for electrons
D_p	Diffusion Coefficient for holes
d	Depletion layer width
d_n	Thickness of n-type layer in BCCD
d_{ox}	Thickness of oxide layer
d_{ox}^{tr}	Thickness of oxide layer of transfer gate
d_{ox}^{st}	Thickness of oxide layer of storage gate
f	Frequency
f_c	Clock frequency
$f_{c/2}$	Nyquist frequency
g_m	Instantaneous transconductance
g	Reverse transfer conductance
H	Feedback coefficient
h_K	Weighting factor in transversal filter
I	Current
I_s	Signal Current
J	Current density
J_p	Hole current density
J_n	Electron current density
J_{nd}	Dark electron current density

K	Feedback Coefficient
k	Boltzmann's constant
L	electrode length
L_b	Length of stage in contact with bias charge (FAT ZEROS)
L_s	Length of stage in contact with signal charge
L_{st}	Length of storage electrode
L_{tr}	Length of transfer electrode
M	Number of parallel channels
N	Number of elements Unit Cells
N_A	Acceptor concentration
N_D	Donor Concentration
N_{eq}	$(1/N_A + 1/N_D)^{-1}$
N_{ss}	Interface state density
N_t	Concentration of bulk traps
n	Electron concentration. Also number of stages in a CCD
n_i	Electron concentration in intrinsic S_i
n'_s	Number of signal electrons in a given well
p	Number of phases
Q	Charge per unit area
Q^+	Total charge per packet
Q_B	Bound charge per unit area in acceptor states in transition region
Q_d	Dark charge in the i'th well
Q_G	Net charge per unit area in gate
Q_{in}	Input charge per unit area
Q_n	Mobile charge per unit area (free electrons) in potential well

Q_n	Mobile charge in potential well
$Q_{n \max}$	Maximum charge per unit area that well can accept
Q_{nB}	Charge handling capacity of BCCD
Q_{nS}	Charge handling capacity of SCCD
Q_o'	Initial sending charge
Q_s	Net charge per unit area in Si
Q_s'	Net charge in Si in potential well area
Q_{ss}	Surface state charge per unit area
$R(f)$	Frequency response function
R_n (R_p)	Net recombination rate of electrons (holes)
T	Time delay
T_C	Time delay of each element in a transversal filter
T_{tr}	Carrier transfer time
$t_{f \min}$	Minimum fall time
t_{TR}	Single carrier transfer time
t_o	Time constant associated with self-induced drift
V	Voltage: Normally with respect to Si substrate
ΔV	Voltage difference between adjacent electrodes
V_{FB}	Flat-band potential: The value of V_G required for $\phi_s = 0$
V_{FG}	The voltage on the floating gate
V_G	The voltage on the gate
V_H	The "high" voltage on an electrode
V_L	The "low" voltage on an electrode
V_t	Voltage across p-n junction required no deplete channel in BCCD

V_P	Magnitude of voltage of clock pulse
V_R	"rest" voltage
V_{ref}	Reference voltage
V_s	Volume of signal charge
V_{sig}	Signal voltage
V_T	Threshold voltage
W	Width of channel in BCCD
W_b	Width of stage in contact with bias charge
W_s	Width of stage in contact with signal charge
δ	Fixed charge loss per transfer
Δ	Fixed charge loss per transfer
ϵ	Transfer inefficiency ($1-\eta$)
ϵ_{ox}	Permittivity of SiO_2
ξ	Electrostatic field
ξ_{fmin}	Minimum fringing field along channel
ϵ_i	Intrinsic transfer inefficiency
ϵ_n	Transfer inefficiency at Nyquist frequency
ϵ_s	Permittivity of Si
ξ_y	Self-induced electrostatic field along channel
η	Transfer efficiency
ϕ	Electrostatic potential. Also designates phase
ϕ_b	Barrier potential
ϕ_{ch}	Channel potential
ϕ_f	Electrostatic potential between intrinsic and extrinsic Fermi level

ϕ_{ms}	Work function between gate and substrate
ϕ_{ox}	Potential across oxide
ϕ_{pn}	Equilibrium barrier height of p-n junction
ϕ_s	Surface potential with respect to bulk Si
ϕ_{sd}	Drain surface potential
ϕ_{sdo}	Surface potential at drain for zero charge
ϕ_{ss}	Source surface potential
ϕ_{sso}	Source surface potential for zero charge
τ	Minority carrier lifetime. Also thermal time constant
τ_e	Emission time constant
τ_f	Final time constant
τ_n	Electron lifetime
μ_n	Electron mobility
μ_p	Hole mobility
$\omega(f)$	Frequency response of transversal filter

2. FUNDAMENTAL CHARGE-COUPLED DEVICE PRINCIPLES AND IMPLEMENTATIONS

2.1. The MOS Capacitor

2.1.1. Qualitative description. The basic element of a CCD is the metal-oxide-semiconductor (MOS) capacitor. The theory of MOS interfaces and capacitance is discussed in detail in several references (e.g. 10,11) so the discussion presented here is limited to the pertinent results of the theory and its extension to CCD structures. The theory is illustrated by the use of n-channel devices unless specifically stated otherwise. The operation of p-channel devices is identical to that of the n-channel devices with the exception of the polarities of the applied voltages and internal potentials, and the sign of the charge carriers. A linear array of MOS capacitors is shown schematically in Fig. 2.1. A capacitor consists of a metal plate (gate) deposited onto a SiO_2 layer which was thermally grown onto a p-type Si substrate. With positive voltage applied to the metal plate with respect to the substrate, the majority carriers in the silicon, holes in this case, are repelled from the surface, and a depletion region is formed in the silicon under the electrode. For sufficiently large voltages, the energy bands in the silicon at the silicon-oxide interface are bent such that an inversion region is formed. A Si interface is said to be inverted if the Si conduction band edge E_c at the Si- SiO_2 interface is at a low enough potential such that in the steady state condition its electron density is comparable to, or greater than, the hole density in the bulk of the substrate. Figure 2.2 shows schematically the situation for gate voltage, V_G , applied such that inversion exists. Figures 2.2a and 2.2b represent the case in which no carriers are present in the conduction band at the interface. Figure 2.2a shows a hybrid schematic diagram of the structure on a plane normal to the surface of the gate. Superimposed onto this diagram is a "well" or "bucket" representing the energy from the Fermi level in the bulk Si to the bottom of the conduction band at the Si- SiO_2 interface. This can be seen by a comparison of Fig. 2.2a with Fig. 2.2b, an energy band diagram through the gate normal to the surface.

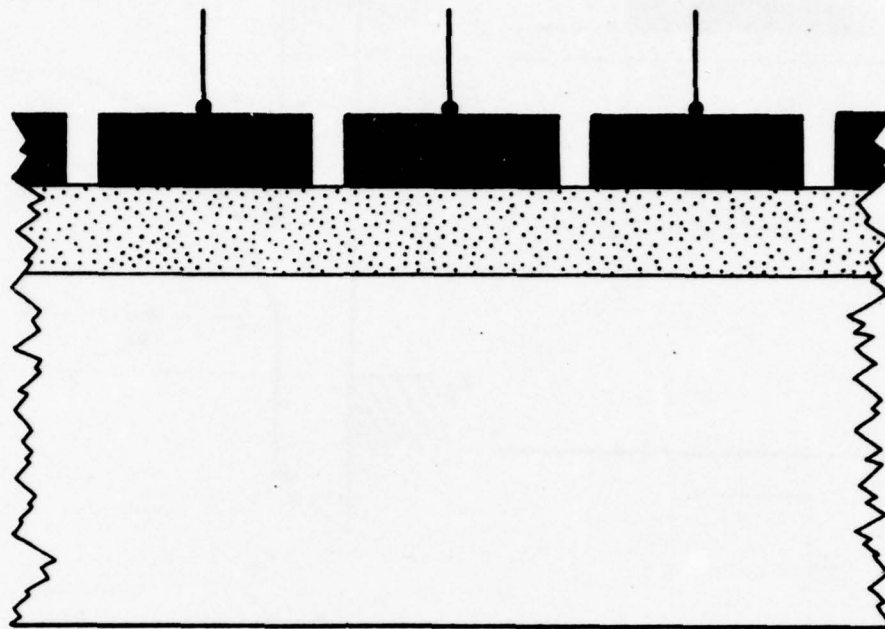


Figure 2.1. Schematic diagram of an array of MOS capacitors

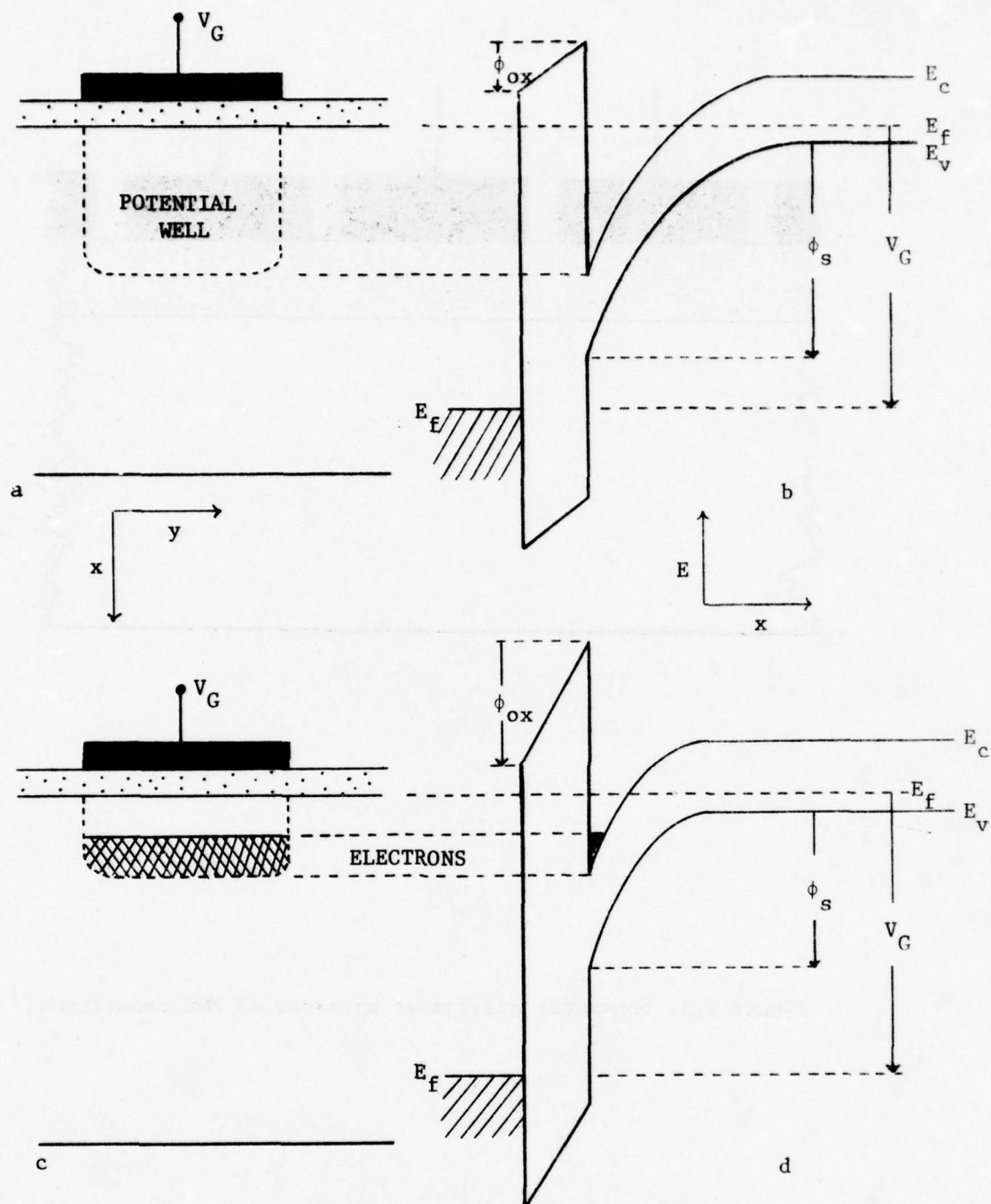


Figure 2.2. Hybrid and energy band diagrams of a MOS capacitor for positive electrode voltage V_G with respect to Si substrate. In a and b the potential well is empty. In c and d electrons are in the well.

Figures 2.2c and 2.2d show the corresponding hybrid and energy band diagrams for the capacitor with the same gate voltage but with electrons present in the conduction band. Note that the presence of this charge increases the potential energy of the interface region, and since V_G is fixed, the increase in potential drop on the oxide ϕ_{ox} relative to that for Figs. 2.2a and 2.2b is equal to the decrease in potential drop in the Si ϕ_s . The electrons in the conduction band or in the well are indicated in the hybrid schematic. Note that the well represents position horizontally vs potential energy vertically. The electrons in the bottom of the well are located within approximately 10nm of the Si-SiO₂ interface and within a few hundredths of an eV from the bottom of the well. For visual clarity, this extent of occupation of the well is exaggerated with respect to the total depth of the well (eV). The doping level in the Si substrate affects the potential dropped across the oxide relative to that across the Si depletion region. For a given oxide thickness and gate voltage, an increase in substrate doping level increases the potential across the oxide and reduces the depth of the potential well. This is illustrated schematically in Fig. 2.3 where the p-type doping concentration is increased in the regions indicated (by diffusion or ion implantation). The depth of the potential well is greatest where the substrate doping (at the surface) is the lightest. As will be seen later, such selective doping of the substrate is used to shape the potential well profiles.

In operation of a CCD, electrons are collected in these wells. The electrons may be generated in the Si by incident photons and captured by the potential well as in an image sensor, or may be transferred between adjacent wells as in a shift register. In addition, electrons can be generated thermally. Since thermal generation is a relatively slow process (10^{-2} - 10^1 seconds to fill the well) any processing of signal charge must be done in a time which is short compared to the thermal generation time.

2.1.2. Quantitative description of MOS capacitor. It is useful to have an expression relating the applied gate voltage V_G , the mobile electron

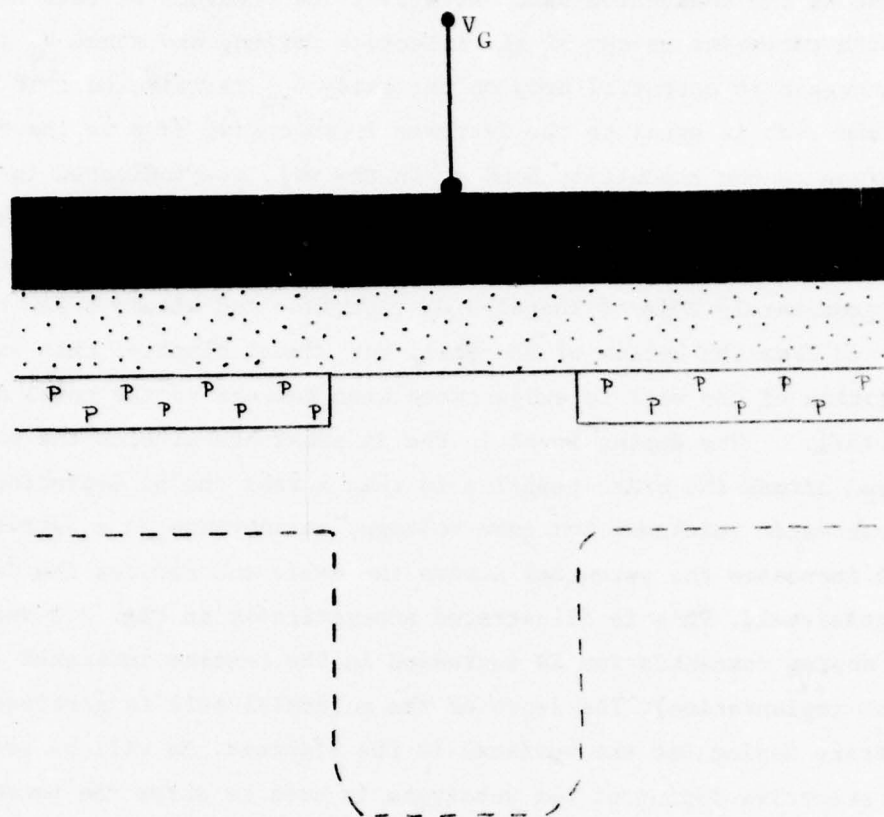


Figure 2.3. The potential well is profiled by the selective use of regions of higher substrate doping levels

charge per unit area in the well Q_n , the surface potential ϕ_s , and the material properties of the MOS capacitor. The derivation is outlined in this section under certain simplifying assumptions:

Assumptions

- i) The substrate impurity density N_A , is uniform
- ii) The surface state density N_{ss} is immobile and independent of V_G and Q_n
- iii) The voltage drop across the inversion layer is negligible compared to that across the depletion region
- iv) The width of the inversion region is negligible compared to the depletion layer width

Definitions of terms and symbols

The terms and symbols which are used are defined below and with reference to Fig. 2.4. Applied voltage is denoted by V , while ϕ represents electrostatic potential differences.

Inversion Layer: that region in which the steady state condition minority carriers are present in concentration greater than that of majority carriers in the bulk.

Depletion Region: that region in which the mobile carrier density is negligible compared to that of the majority carrier density in the bulk.

V_G , Gate Voltage: the voltage applied to the gate with respect to the substrate.

$V_T = 2\phi_f$, Threshold Voltage: the gate voltage required to create an inversion layer in the steady state case.

$\phi_f = E_i - E_f$: the electrostatic potential between the Si intrinsic Fermi level E_i and the Fermi level E_f in the bulk.

ϕ_s , Surface Potential: the voltage of the Si-SiO₂ interface with respect to the bulk Si.

$V_{FB} = \phi_{ms} - Q_{ss}/C_{ox}$, Flat Band Potential: the value of V_G required to reduce ϕ_s to zero, i.e. to flatten the bands in the Si.

Q_{ss} , the Surface State Charge Density Per Unit Area: the charge residing in the SiO₂ very near the SiO₂/Si interface. It is found to be non-mobile and positive.

ϕ_{ms} , Work Function difference between metal and semiconductor.

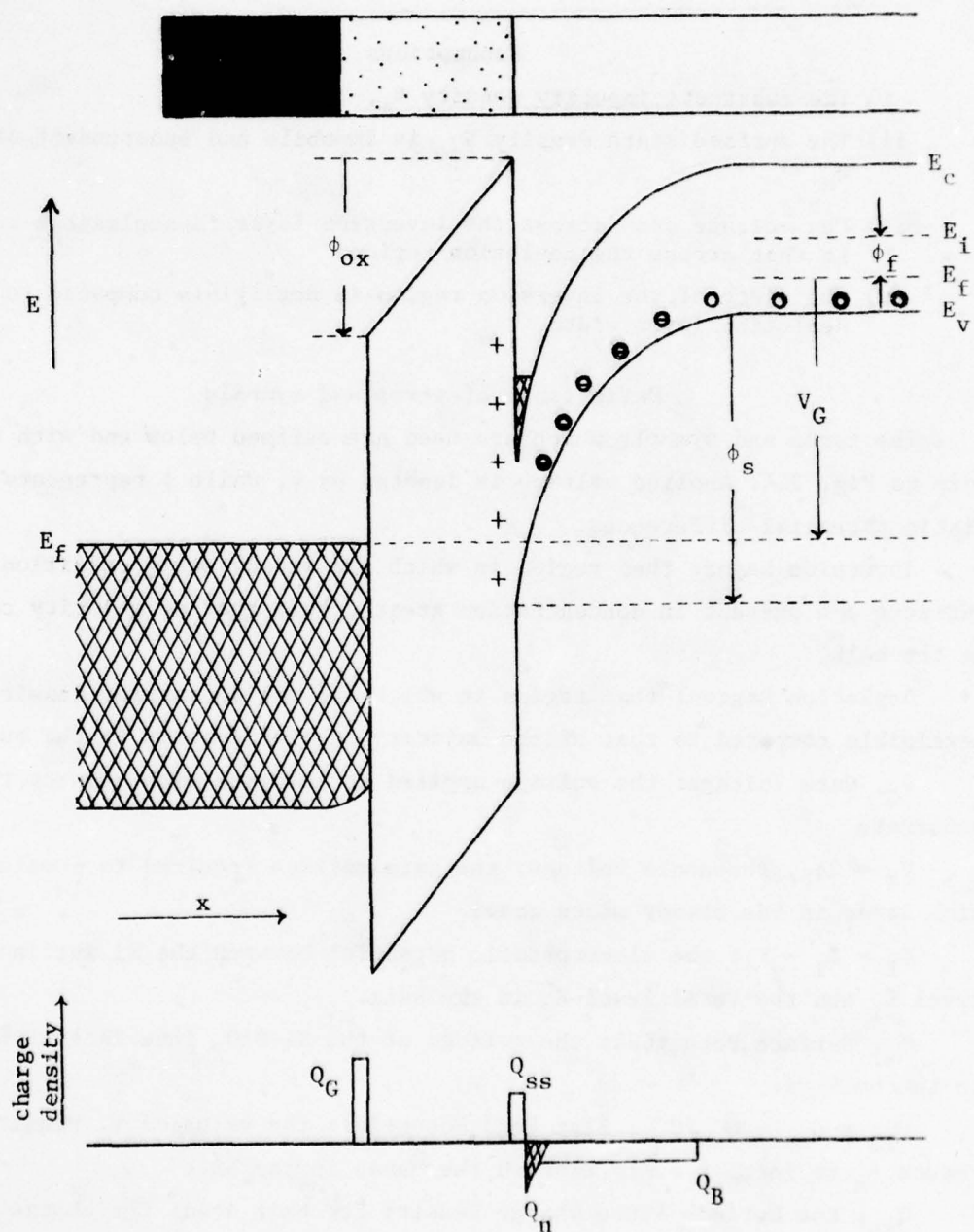


Figure 2.4. Illustration of quantities used for analyses of MOS capacitor

$$C_{ox}, \text{Oxide Capacitance Per Unit Area: } Q_G / \phi_{ox} = -\frac{(Q_s + Q_{ss})}{\phi_{ox}} = \epsilon_{ox} / d_{ox}$$

ϕ_{ox} : the electrostatic potential across the oxide, or the electrostatic potential of the gate with respect to the Si surface.

Q_G : the net charge per unit area on the gate.

$Q_s = Q_n + Q_B$: the net charge per unit area in the Si.

Q_n : the mobile charge (electrons) per unit area in the inversion layer.

Q_B : the bound charge per unit area in acceptor states in the transition region.

d_{ox} : thickness of SiO_2 .

ϵ_s : electrical permittivity of Si.

ϵ_{ox} : electrical permittivity of SiO_2 .

$x_d = (2\epsilon_s \phi_s / qN_A)^{1/2}$: depletion region width.

We first show that the (differential) capacitance between gate and substrate bulk C_{GB} can be expressed as the series combination of the oxide capacitance C_{ox} and the depletion capacitance in the Si, C_D .

By definition

$$C_{GB} = \frac{dQ_G}{dV_G} \quad (2.1)$$

Since the net charge in the capacitor is zero,

$$Q_G = -(Q_{ss} + Q_n + Q_B).$$

Since Q_{ss} and Q_n are assumed independent of V_G ,

$$C_{GB} = -\frac{dQ_B}{dV_G}. \quad (2.2)$$

The gate voltage can be expressed

$$V_G = V_{FB} + \phi_s - \frac{Q_n}{C_{ox}} - \frac{Q_B}{C_{ox}}, \quad (2.3)$$

and since V_{FB} and Q_n are constant

$$dV_G = d\phi_s - \frac{dQ_B}{C_{ox}}. \quad (2.4)$$

Substituting Eq. 2.4 into Eq. 2.2 gives

$$C_{GB} = \frac{1}{1/C_{ox} - d\phi_s/dQ_B}$$

Since $C_D = -dQ_B/d\phi_s$, where C_D is the capacitance per unit area of the depletion region,

$$C_{GB} = \frac{1}{1/C_{ox} + 1/C_D} \quad (2.5)$$

or C_{GB} is equal to the series capacitance of C_{ox} and C_D . It is convenient to express Eq. 2.5 as

$$\frac{C_{GB}}{C_{ox}} = \frac{1}{1 + C_{ox}/C_D} \quad (2.6)$$

We next derive an expression for ϕ_s . Using the depletion approximation, $Q_B = (2qN_A\epsilon_{ox}\phi_s)^{1/2}$ and Eq. 2.3 becomes

$$V_G = V_{FB} + \phi_s - \frac{Q_n}{C_{ox}} - \frac{(2qN_A\epsilon_{ox}\phi_s)^{1/2}}{C_{ox}} \quad (2.7)$$

Solving Eq. 2.7 for ϕ_s yields

$$\phi_s = V_G - V_{FB} + \frac{Q_n}{C_{ox}} + \frac{qN_A\epsilon_{ox}}{C_{ox}^2} - \left[\frac{2qN_A\epsilon_{ox}}{C_{ox}^2} \left(V_G - V_{FB} + \frac{Q_n}{C_{ox}} \right) + \left(\frac{qN_A\epsilon_{ox}}{C_{ox}^2} \right)^2 \right]^{1/2} \quad (2.8)$$

Letting

$$V'_G \equiv V_G - V_{FB} + \frac{Q_n}{C_{ox}} \quad \text{and}$$

$$V_0 = \frac{qN_A\epsilon_s}{C_{ox}}$$

Eq. 2.8 can be written

$$\phi_s = V'_G + V_0 - [2V'_G V_0 + V_0^2]^{1/2} \quad (2.9)$$

Eq. 2.6 can then be expressed

$$C_{GB} = \frac{C_{ox}}{1 + (\phi_s/2V_0)^{1/2}} \quad (2.10)$$

Although it is not obvious from Eqs. 2.7 or 2.8, for a given value of V_G as Q_n increases ϕ_s decreases and thus from Eq. 2.10, C_{GB} increases. This is as expected, since as ϕ_s decreases so does the depletion width x_d

$$x_d = \left[\frac{2\epsilon_s \phi_s}{qN_A} \right]^{1/2}$$

and since

$$C_D = \frac{\epsilon_s}{x_d},$$

C_D and thus C_{GB} increase.

Figure 2.5 shows a graphical interpretation of these equations. We define $Q_{n \max}$ as the maximum charge per unit area that a potential well can accept. If more charge is injected, the depth of the well decreases until ϕ_s becomes so small that the charge spills out into the substrate. In the limiting case for $\phi_s = 0$, we obtain from Eq. 2.7

$$Q_{n \max} = -C_{ox}(V_G - V_{FB})$$

but since V_G is normally much larger than V_{FB} ,

$$Q_{n \max} \approx -C_{ox} V_G \quad (2.11)$$

For $V_G = 10$ volts and $d_{ox} = 100$ nm, $Q_{n \max}$ is on the order of 2×10^{12} electrons/cm². The magnitude of V_G is limited by either the avalanche breakdown voltage of the substrate or the oxide rupture voltage, whichever is the smaller.

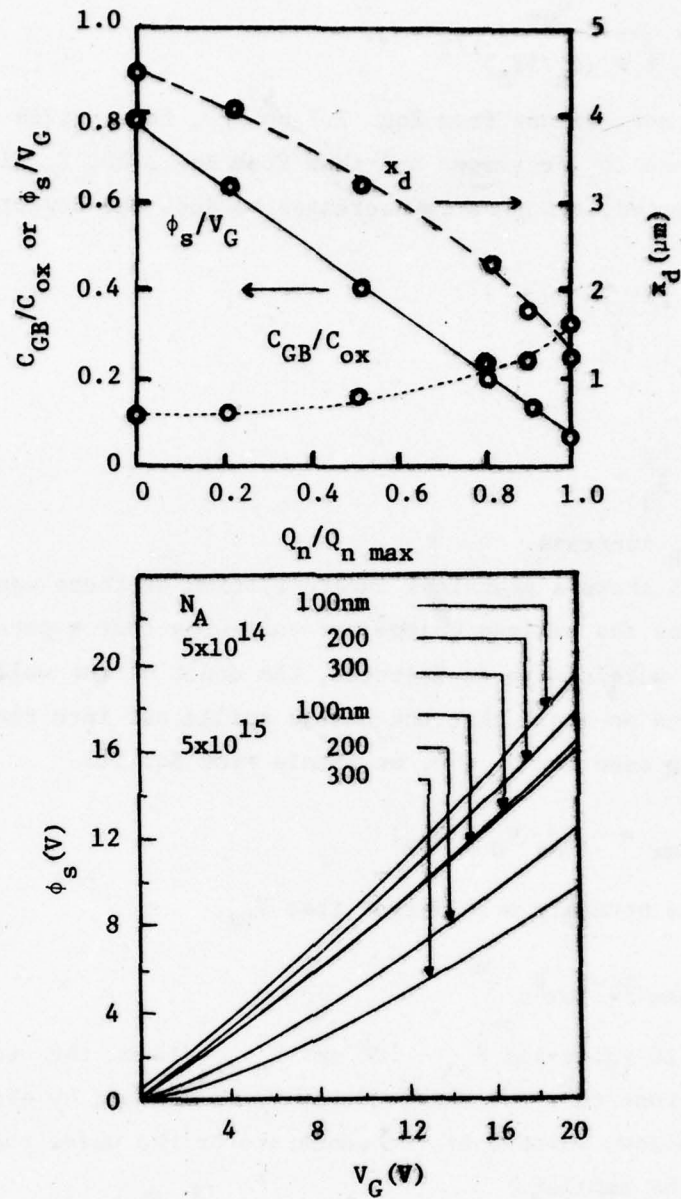


Figure 2.5. Functional dependence of surface potential (after 6 and 9).

2.2. Basic CCD Structures

CCD's can be classified as surface channel charge-coupled devices (SCCD's) or bulk channel charge-coupled devices (BCCD's) depending whether the charge is transferred at the Si surface^{*} or within the bulk of the Si substrate.

2.2.1. Surface channel charge-coupled devices (SCCD's). An SCCD in its simplest form consists of a linear array of MOS capacitors fabricated on an oxidized p-Si substrate of uniform doping as shown in Fig. 2.1. The hybrid schematic of a single stage of a three-phase SCCD is shown in Fig. 2.6 to illustrate the process of charge transfer. The capacitor gates are pulsed sequentially to form potential wells and the electrons move along the surface by flowing from one well into an adjacent well which is deeper, i.e., it has a more positive gate voltage. The wells must be closely spaced so that fringing fields from gate to substrate reduce the potential energy between the wells sufficiently to permit electron flow. In Fig. 2.6a a signal charge is represented as being in the potential well under the first electrode while the other two electrodes are biased to a quiescent point just beyond threshold. In b, the potential has been reduced on the first well while the potential applied to the second electrode creates a deep potential well and electrons tend to flow to the deeper well. In c, the charge has been transferred to the second well and the voltage on the first electrode has been reduced to its quiescent value. The charge has made one complete transfer but it has moved only one-third of a stage. It is to be noted here that the surface potential, or the depth of the well depends on the charge present. This is indicated by a reduction of the depth of the second well from b to c as the charge transfers. It is to be noted in b, which represents the conditions during transfer, that the first well is shallower on the left than on the right because of the different charge densities. This creates an electric field ξ_y , along the surface in

* Hereafter, the terms Si surface, or simply surface, will refer to the Si/SiO₂ interface.

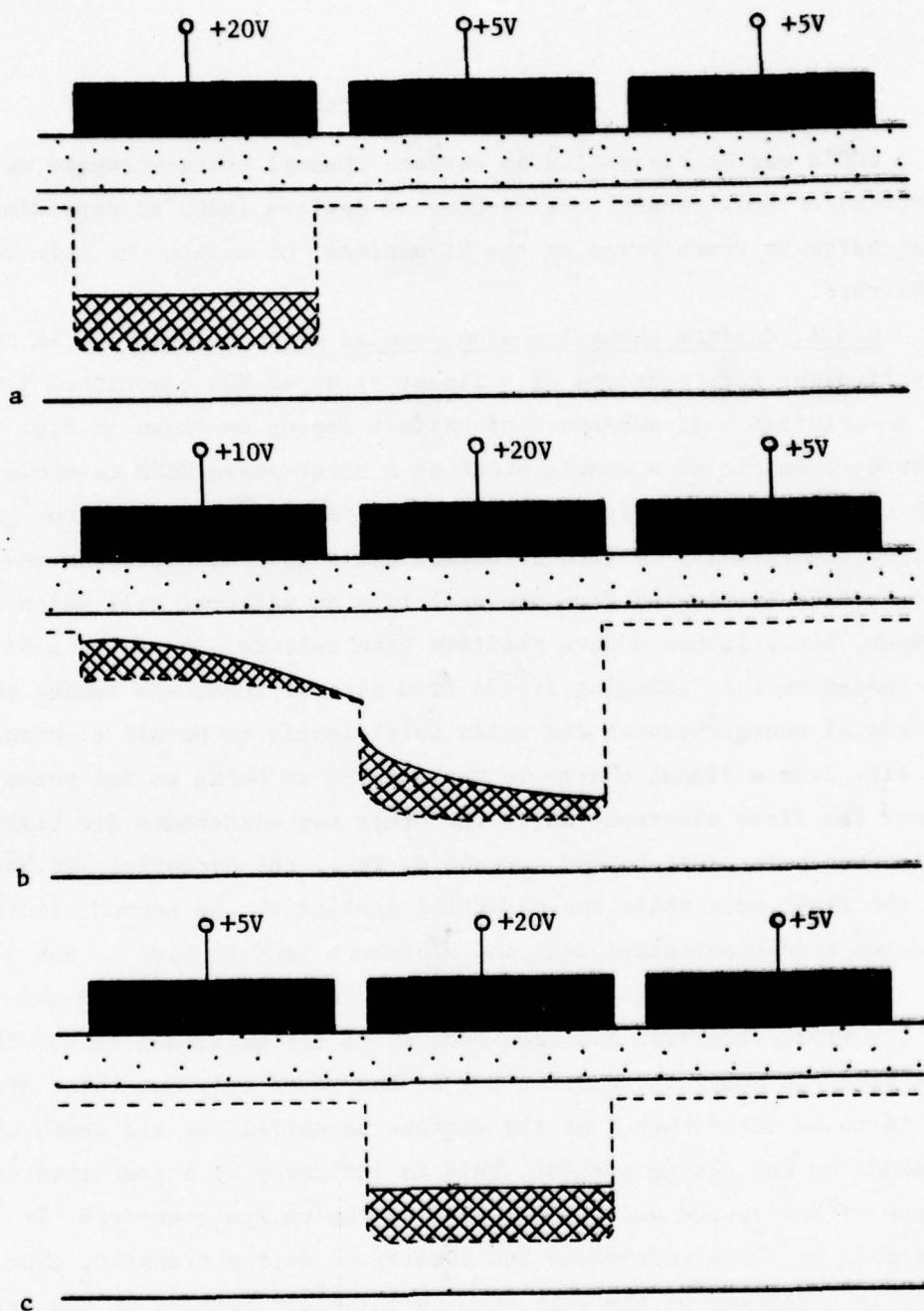


Figure 2.6. Hybrid schematic illustration of charge transfer (see Text)

the direction to aid in the charge transfer where

$$\xi_y = - \frac{1}{q} \frac{d\phi_s}{dy}$$

2.2.2. Bulk channel charge-coupled devices (BCCD's). In BCCD's the potential well minima occur within the Si bulk so that the mobile electrons are not in contact with the Si/SiO₂ interface. This tends to increase the electron mobility, increase ξ_y by creating fringing fields, and thus decrease the transfer time, as discussed later. It also eliminates trapping of the signal electrons at the interface states. BCCD's are also referred to as "buried channel CCD's" (12,13) and "peristaltic CCD's" (14). Figure 2.7 shows three common structures of BCCD's. As shown in Fig. 2.7a, one form utilizes a homogeneous n-doped epitaxial layer about 4-5 μm thick and a net donor concentration on the order of $7 \times 10^{14} \text{ cm}^{-3}$. To increase the charge carrying capabilities the donor concentration is often "profiled" such that the maximum donor concentration occurs at the Si interface. This can be accomplished by ion implantation of phosphorus followed by a high temperature drive-in diffusion. The resultant impurity distribution is approximately Gaussian with a total n-layer thickness on the order of 4.5 to 5 μm and surface donor concentration of $5 \times 10^{15} \text{ cm}^{-3}$ to $2 \times 10^{16} \text{ cm}^{-3}$ (2,15-17). This requires a phosphorus implant dose of approximately $1 \times 10^{12} \text{ ions/cm}^2$. Alternately, profiled BCCD's have been fabricated as shown in Fig. 2.7c using an n-doped epitaxial layer with a net donor concentration on the order of $3 \times 10^{14} \text{ cm}^{-3}$. The surface donor density is increased by ion implantation of phosphorus to a depth of 0.5 μm using a dose of $5 \times 10^{11} \text{ ions/cm}^2$.

Under normal operation, BCCD's require a positive voltage applied to the n-regions with respect to gate and to substrate of sufficient magnitude to completely deplete the n-region. Figure 2.8 shows the energy band diagram through a gate of the contoured BCCD of Fig. 2.7b without bias (a), with bias but without charge (b) and with bias and with charge (c). With

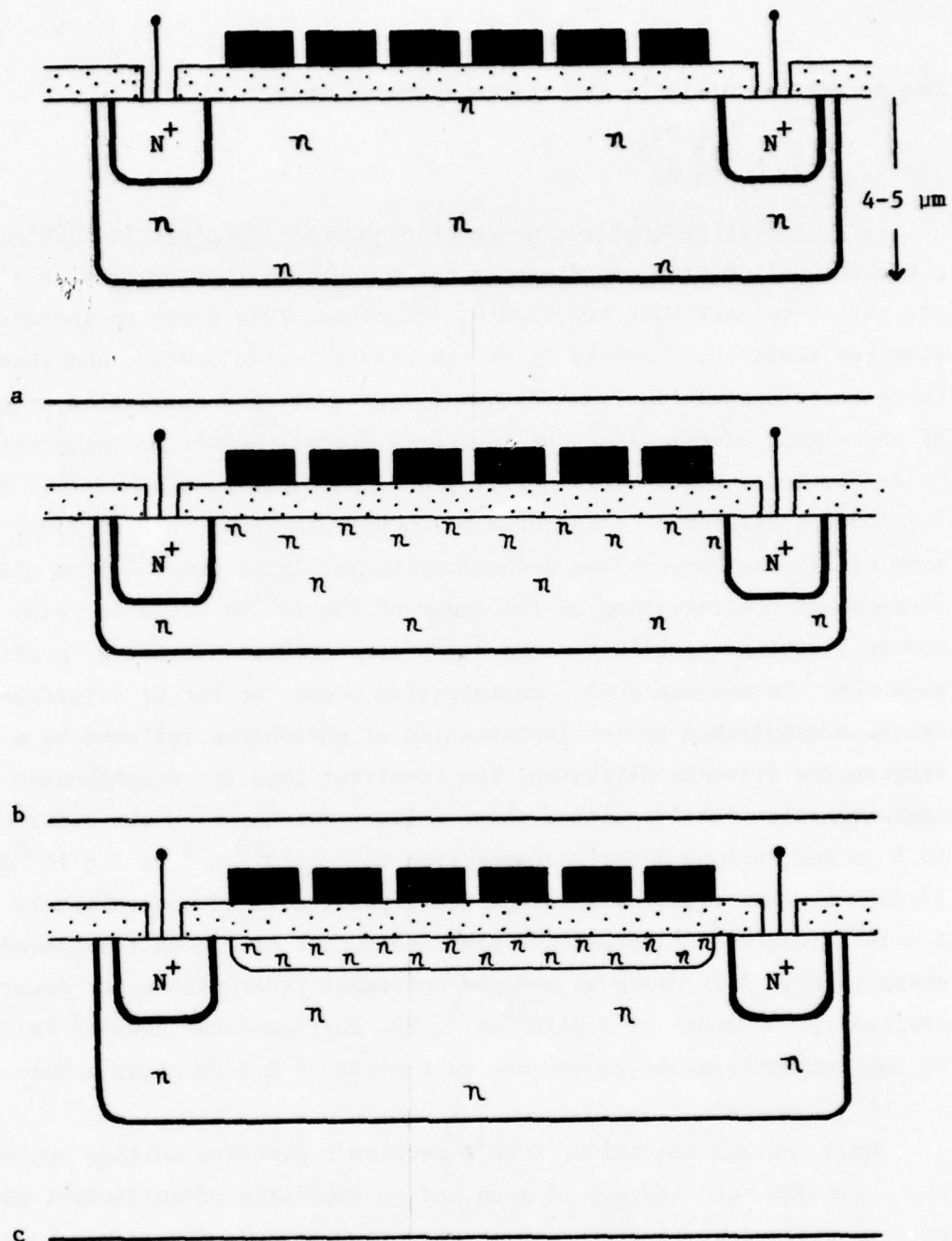


Figure 2.7. Bulk channel CCD structures using a) homogeneous n-type epitaxial layer, b) ion-implanted layer and c) a combination of the two

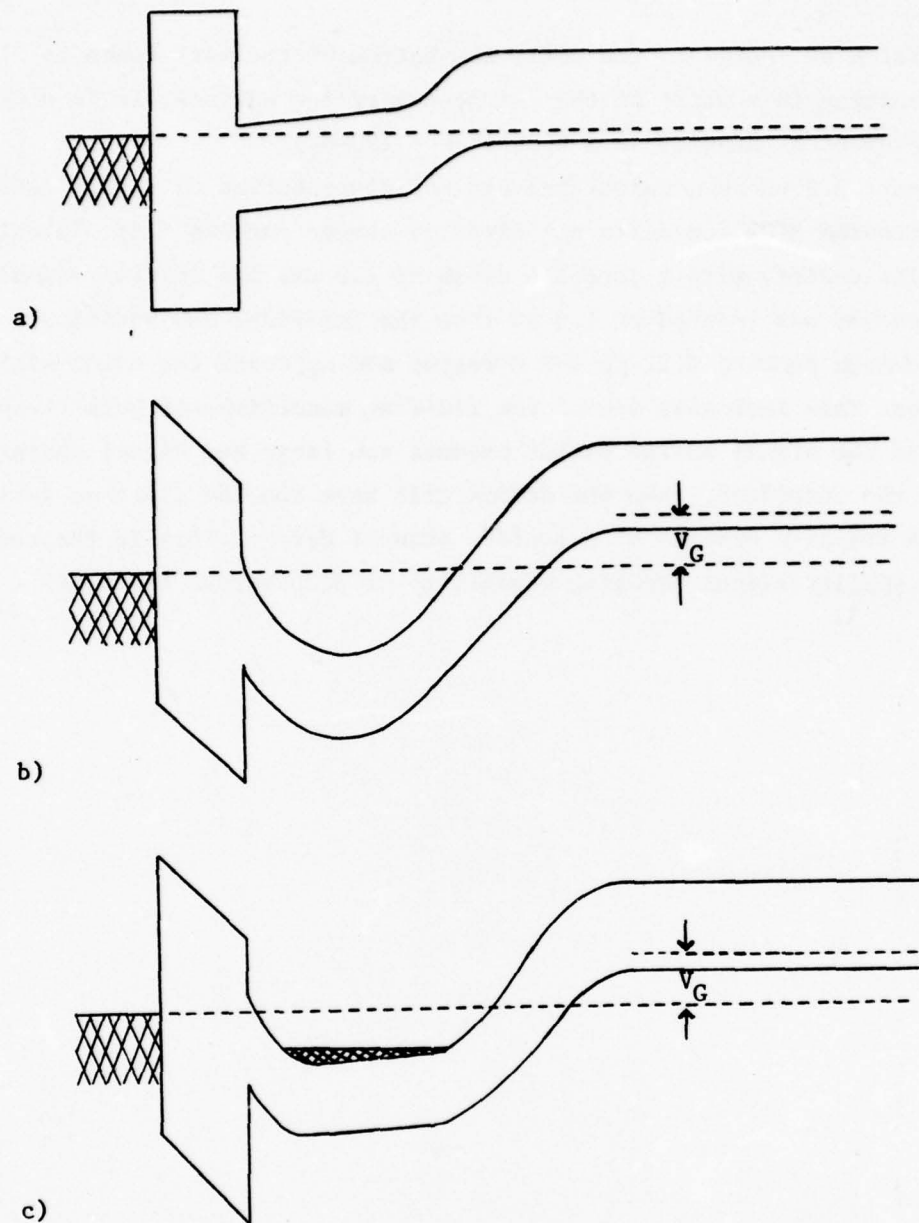


Figure 2.8. Energy band diagrams normal to gate of a contoured BCCD:
a) equilibrium condition, b) with bias applied but with no
signal charge and c) with signal charge present.

the addition of charge in the well, the bottom of the well tends to flatten, resulting in a shift of the charge toward the surface. It is noted that the electron density in a BCCD is $n = (N_D - N_A)$.

Figure 2.9 shows a calculated typical distribution of signal charge in a contoured BCCD for different sizes of charge packets (18). In this particular device, with a junction depth of $2.2 \mu\text{m}$, the initial signal charge packet was located at $1.0 \mu\text{m}$ from the interface and additional signal charge packets fill up the n-region and approach the oxide-silicon interface. This indicates one of the limiting conditions of bulk channel CCD's. If the signal charge packet becomes too large and signal charge reaches the interface, then the device will have the low electron mobility and high trapping problem of a surface channel device. This is the reason for the smaller signal handling capability of BCCD versus the SCCD.

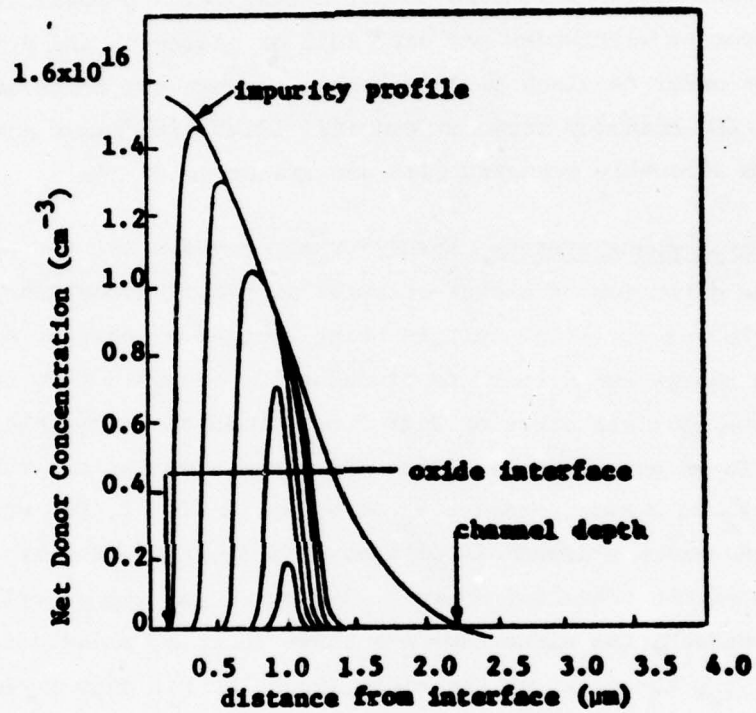


Figure 2.9. Distribution of various sized charge packets in a contoured BCCD for a specific (Gaussian) donor concentration distribution (after 18)

2.3. Transfer Electrode Structures

As indicated earlier, a CCD is basically an analog delay line in which charge is transferred along a channel created by pulsing a series of transfer electrodes with properly phased voltages. Many transfer schemes have been proposed involving one-to-four-phase systems with a variety of electrode structures. In practice, however, two-phase and three-phase systems are used predominantly. It should be noted that for a p -phase system, there are p storage electrodes per unit cell or elements, and p transfers per unit cell. In order to clock signal charges through the cells at clock frequency f_c , the transfer rate between individual electrodes must be pf_c or the maximum allowable transfer time per electrode is $1/pf_c$.

2.3.1. Three-phase systems. Three-(or more)-phase systems are required to control the direction of charge-transfer if simple symmetrical electrodes are used. While one potential well is being emptied of charge, another is receiving the charge and a third is blocking the backward flow of charge. The three-phase (3ϕ) structure of Fig. 2.6 is used as an example in Fig. 2.10 (19,9). To be specific, we assume the three clock pulses vary from a rest voltage V_R to a more positive V_G as shown in Fig. 2.10e, where the negative of the clock voltages is plotted as a function of time (to agree with the sign of the potential energy). The potential energy wells for electrons underneath the electrodes are shown in a, b, c and d respectively for times t_1 , t_2 , t_3 and t_4 of the clock input. At t_1 , only ϕ_1 is energized and so potential wells exist only under ϕ_1 gates. To emphasize that this is an analog device, we assume that the two potential wells under the ϕ_1 electrodes are occupied with different quantities of charge as shown in a. Note that the depth of the well depends on its quantity of charge Q_n as well as on V_G . At t_2 , both ϕ_1 and ϕ_2 are energized and the charge is divided as shown in b. At t_3 , the voltage on ϕ_1 is reduced. This reduces the depth of the ϕ_1 well and the electrons transfer to the ϕ_2 well as shown in c. At t_4 , the clocks have completed one-third of a cycle. Only ϕ_2 is energized and one transfer is completed. Three such transfers are required to move the

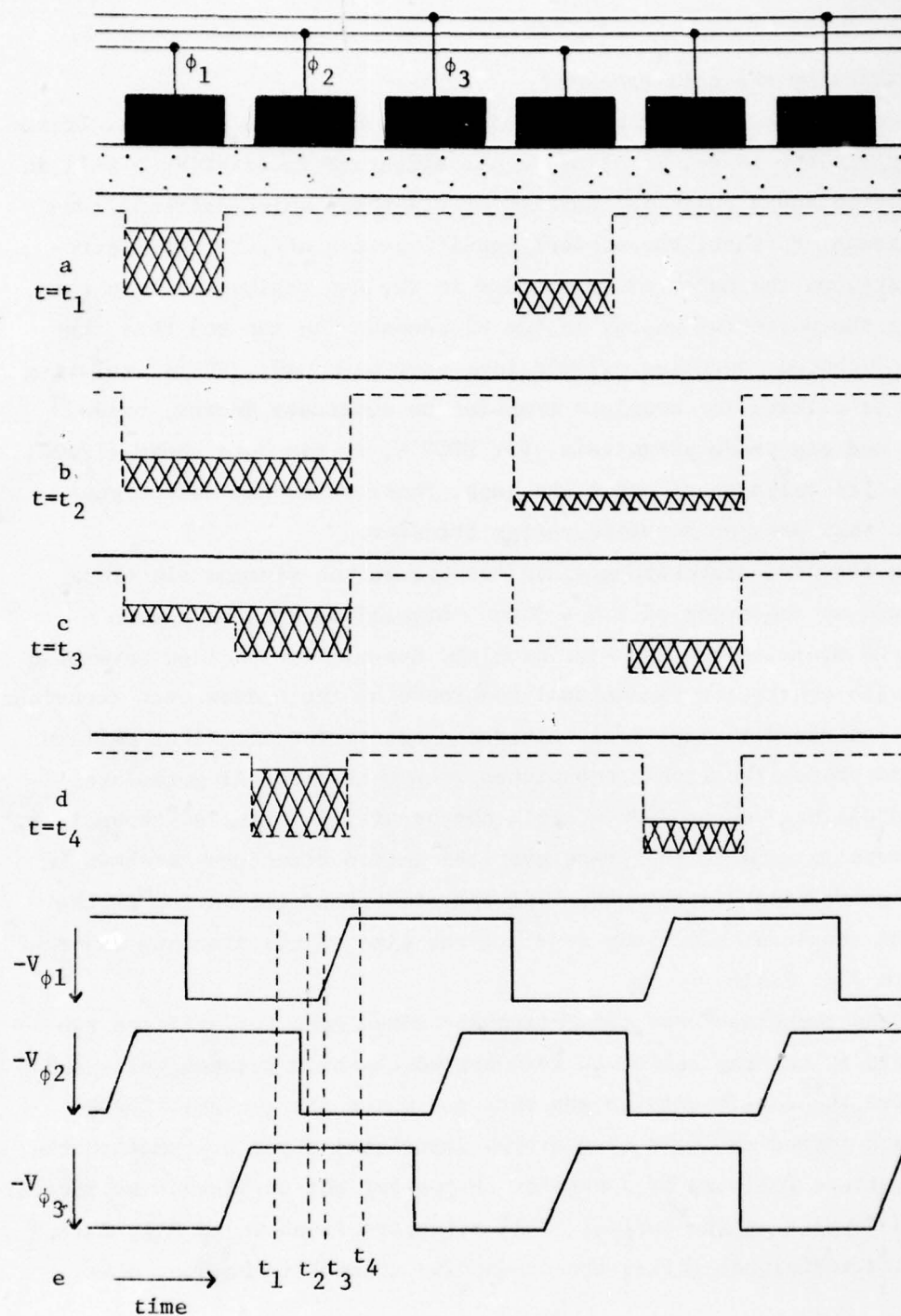


Figure 2.10. Hybrid diagram of a 3- ϕ CCD at different times of a transfer cycle

charge packets by one cell-spacing.

The gaps between the gate electrodes above can cause problems. If the gap spacing is too large, fringing is not effective in creating a well in the gap region and a potential barrier exists there which prevents complete transfer. Further, the ambient conditions can affect the electrostatic charge on the outer oxide surface in the gap region which in turn can affect the potential energy in the Si beneath the gap and thus the transfer of charge. Detailed calculations have been made (20,21) relating the gap size allowed for complete transfer to substrate doping, oxide thickness and electrode potentials. For BCCD's, it has been shown (12,22) that potential wells occur under the gaps. These wells can hold signal charge and thus prevent complete charge transfer.

Using standard photolithographic techniques the minimum electrode spacings are on the order of 2.5 - 3 μm . Several methods have been developed to minimize the gap size problem. Sub-micron spacings have been achieved with consistent dimensional tolerance by the shadow etch technique (23) as illustrated in Fig. 2.11. Alternate electrodes are first defined by standard photolithographic techniques except that the Al gates are overetched slightly to produce a small photoresist overhang as shown in a. A second metalization is then made over the entire structure as shown in b and the photoresist is removed, "lifting off" the metal on top of the resist. The resultant electrode gaps are the size of the aluminum undercut as shown in Fig. 2.11c.

A second technique uses conventionally sized gaps but utilizes two ion implants in the gap region to form buried channels between wells and thus reduces the sensitivity to gap size and oxide charge (24). These channels are formed by implanting n-type impurities about 0.4 μm into the p-type substrate followed by a shallow p-type implant to prevent an inversion layer from forming at the surface. This structure is shown in Fig. 2.12.

A third technique, called the conductive channel technique, uses

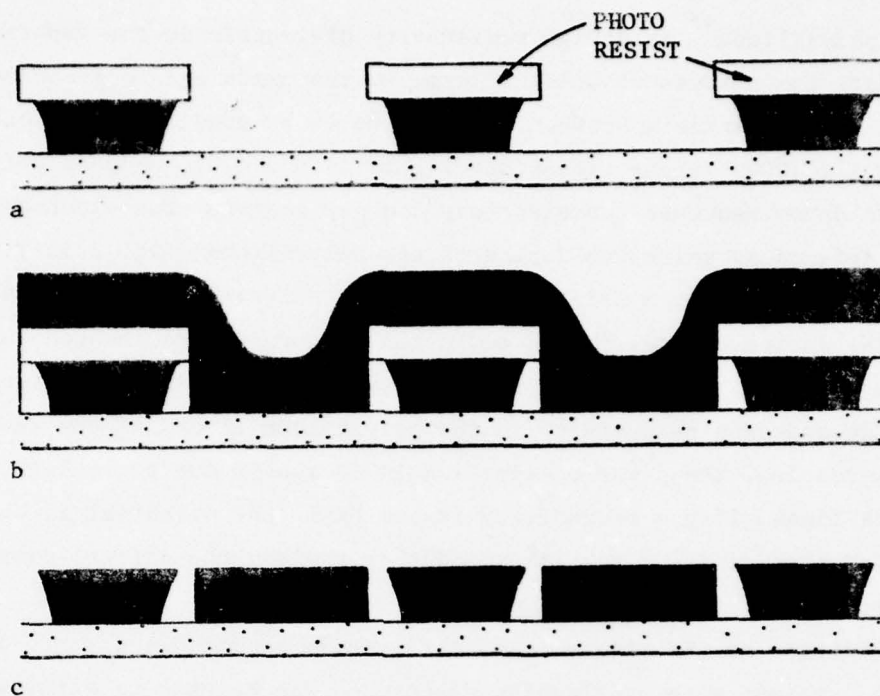


Figure 2.11. Illustration of the shadow etch technique to produce sub-micrometer electrode gaps (see Text)

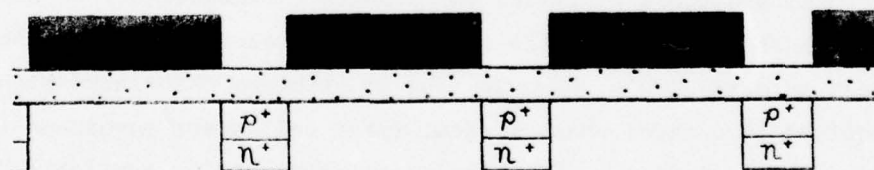


Figure 2.12. A buried n^+ channel is used to couple potential wells and reduce the gap problem (after 24)

undoped* polysilicon** as a high resistivity dielectric in the gap regions to eliminate the effects of static charge on the oxide and to minimize potential energy barriers between adjacent wells by grading the potential between wells (20). In one variation of this method (25), undoped polysilicon is deposited over the electrode and gap regions. The electrodes are then defined by selective doping of the polysilicon (Fig. 2.13a). In another variation (26), a thin (50 nm) undoped polysilicon layer is deposited over the entire channel region and metal electrodes are located on this layer (Fig. 2.13b). One problem with this system is the difficulty in maintaining adequate resistivity in the polysilicon layer. If the resistivity is too low, the power dissipation is increased due to leakage between clock lines. If the resistivity is too high, the potential in the gap lags behind that of the clock lines and thus reduces the effectiveness of this system.

In addition to the single level three-phase techniques described, multilevel systems with overlapping electrodes can be used to eliminate gap size and gap oxide protection problems. One such 3- ϕ system (27) uses three levels of overlapping doped polysilicon as shown in Fig. 2.14. Three different polysilicon deposition and doping operations produce the three sets of electrodes. This structure can be very compact since gaps are effectively eliminated. Utilization of thermally oxidized polysilicon as the electrode insulators minimizes the problem of interelectrode shorts.

Three-phase systems were the first to be developed and were used extensively in early CCD's. However, due to problems associated with crossovers required in a three phase system, large cell space requirements, and clock phasing restrictions, the majority of commercially available CCD's now utilize two-phase systems.

*The term "undoped" indicates that the material is not intentionally doped and is of high resistivity.

**The term "polysilicon", Poly-Si" or simply "poly" is used for "polycrystalline silicon".

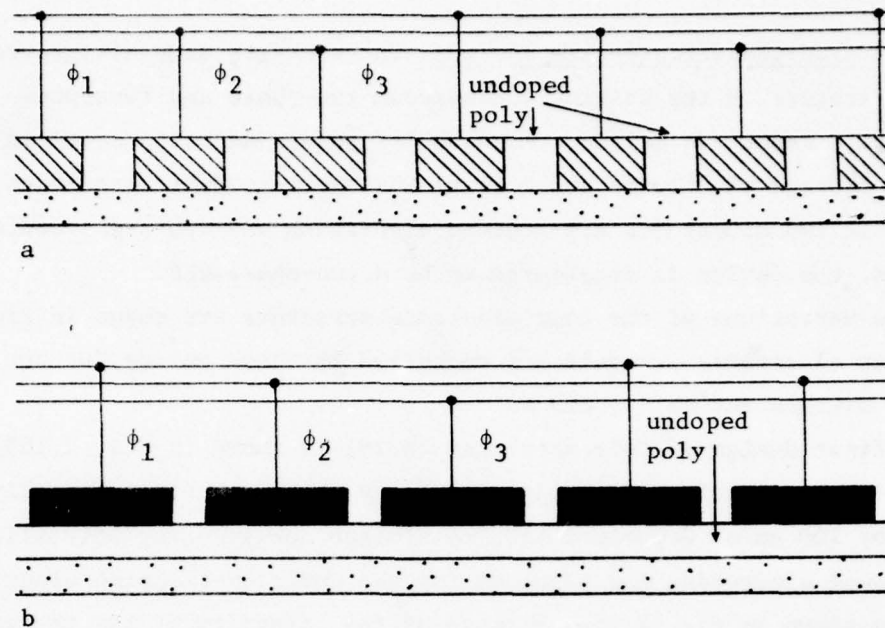


Figure 2.13. Conductive channel techniques a) using undoped poly-Si between doped poly-Si electrodes and b) between metal electrodes and SiO₂

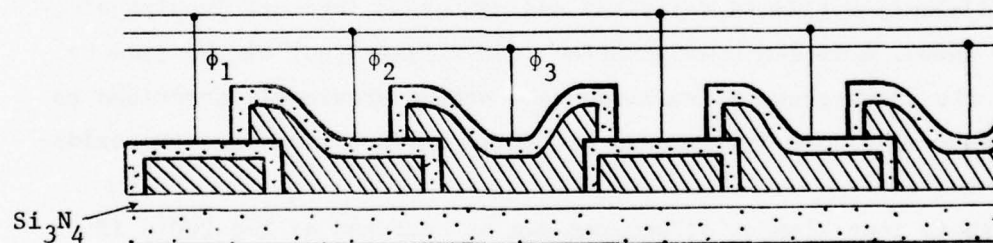


Figure 2.14. System using overlapping doped polysilicon gates. A layer of Si₃N₄ is often used as shown to protect the initial gate oxide from the influence of further processing

2.3.2. Two-phase/four-phase systems. There exists some disagreement in the literature in the distinction between two-phase and four-phase systems. In this report we define the number of phases as being equal to the number of storage electrodes per cell. A CCD may have four electrodes per cell, but if two electrodes are storage electrodes and two are transfer electrodes, the device is considered to be a two-phase CCD.

Three variations of the four electrode structure are shown in Fig. 2.15. If the four electrodes per cell are energized by clock pulses 90° out of phase the devices act as $4-\phi$ CCD's.

The first design of this structure (8,28) is shown in Fig. 2.15a. It contains two levels of overlapping electrodes which are dielectrically isolated by 100 nm of deposited SiO_2 . A similar design using polysilicon for the lower electrodes and aluminum for the upper overlapping electrodes (29-33) is shown in Fig. 2.15b. Because of the integrity of the thermal oxide grown on polysilicon, the system is very reliable and its fabrication is consistent with current MOS processing procedures. A third version of this structure is shown in Fig. 2.15c. It uses aluminum gates with Al_2O_3 insulation between adjacent gates. Alternate Al gates are first defined. These are then anodized. Because the Al_2O_3 thus formed is a good insulator, the second aluminum film is deposited and patterned into overlapping electrodes as shown. A fourth configuration (not illustrated) can be made by modifying the three-phase polysilicon gate scheme previously described to obtain a four-electrode system. Two polysilicon depositions and two oxidations are required.

The above four-element structures can be operated as $2-\phi$ CCD's if assymetry is built into the system so that alternate electrodes are used as storage elements while the remaining electrodes are used to transfer charge from one storage element to another. Consider a $2-\phi$ clock whose lines are connected to the storage elements ϕ_1 and ϕ_3 and a fixed voltage is applied between each storage electrode and its "upstream" transfer electrode. If ϕ_4 and ϕ_2 are made negative with respect to ϕ_1 and ϕ_3 respectively, a longitudinal potential gradient will be set up at the Si

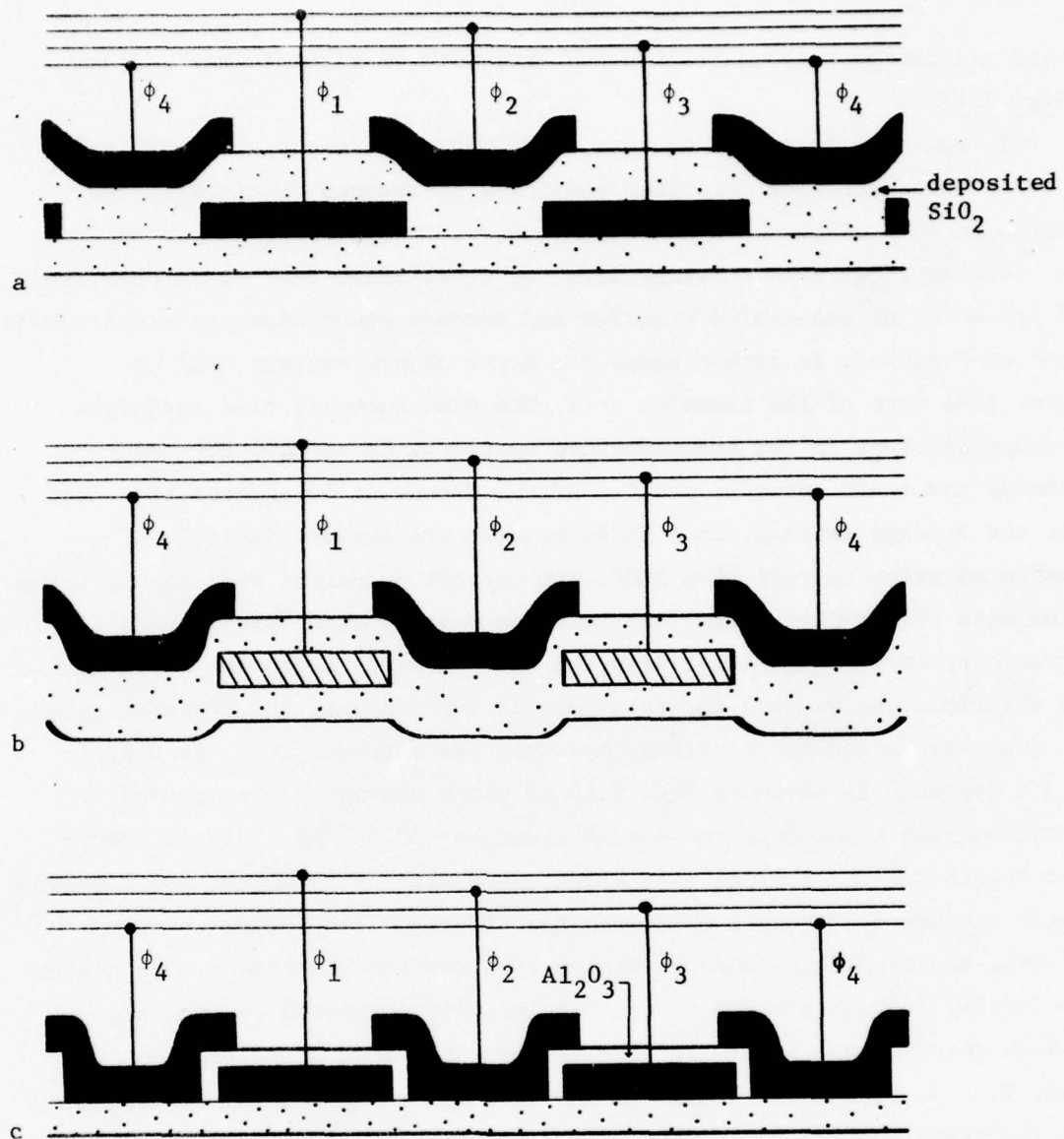


Figure 2.15. Examples of four-phase CCD structures. The depression in the Si in b results from thermal oxidation.

surface and charge will be transferred from left to right in the systems of Fig. 2.15.

This same asymmetry can be established by other means such that only two clock lines are required, thus resulting in savings in clocking complexity. In many of these schemes only two electrodes are used per cell thus reducing total area substantially. In other cases four electrodes are used per cell but associated transfer and storage electrodes are electrically connected together. In either case, the depth of the storage well is greater than that of the transfer well. The most commonly used technique to accomplish this is the stepped-oxide approach. In a SCCD, the oxide thickness under the transfer portion of the electrode is greater than that under the storage section. In a BCCD, because the surface field is of opposite polarity to that of a SCCD, the deepest potential well is under the region with the thicker oxide, and thus the reverse structure is used (15). Alternately, or in combination with the stepped-oxide approach, different gate materials can be used for transfer and for storage, the transfer gate then must have a smaller work function than the storage gate^{*}. An example of this approach is shown in Fig. 2.16 in which storage gates are made of polysilicon, and transfer gates are of aluminum (30,34,35). This is fabricated by growing the initial gate oxide, depositing polysilicon and patterning the storage electrodes, oxidizing the structure (including the polysilicon), and depositing and patterning the transfer electrodes. Associated transfer and storage electrodes are electrically connected on the chip. The work function of the Al (3.2 eV) is less than that of polysilicon (about 4.5 eV, depending on doping) and thus the work function difference aids the stepped-oxide in creating the asymmetry. If additional asymmetry is desired, the depth of the potential well can be reduced in the transfer regions by ion implantation of p-type impurities after the polysilicon patterning (34).

^{*} For an n-channel device. The opposite is true for a p-channel device.

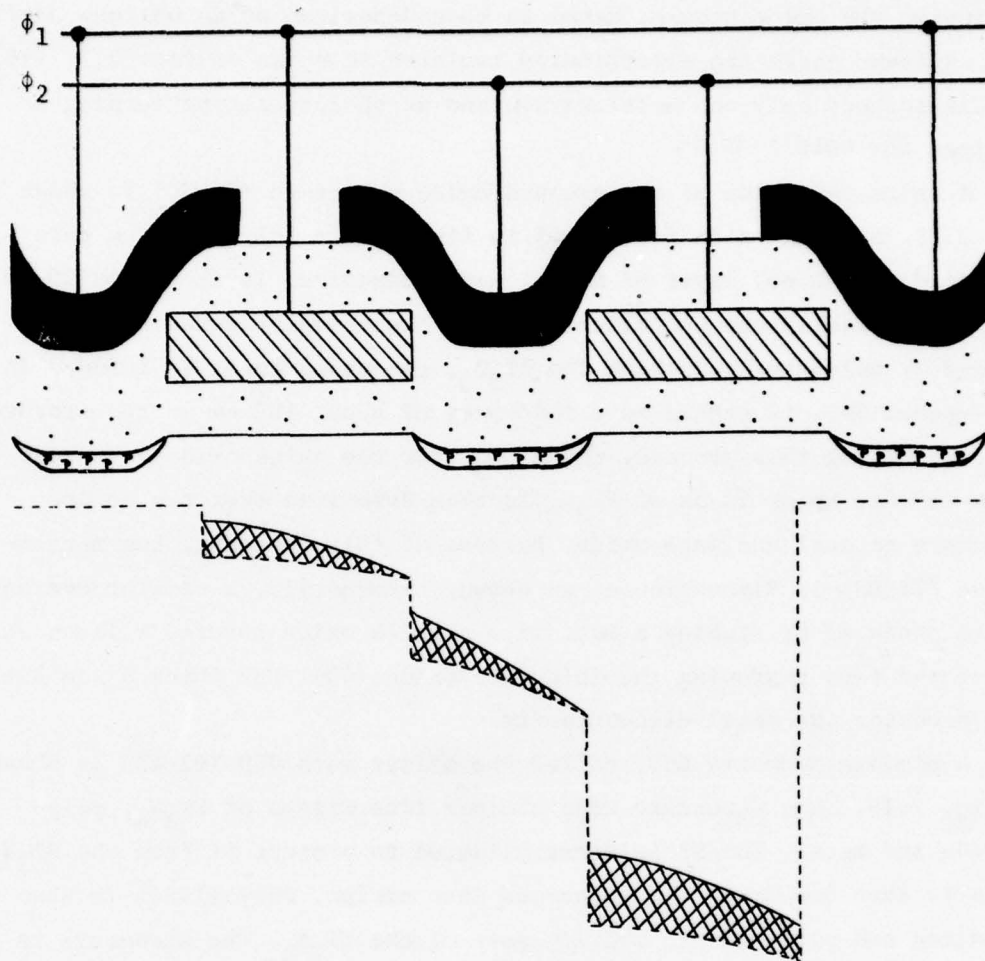


Figure 2.16. Two-phase CCD in which asymmetry is obtained by different oxide thicknesses and different work functions of transfer and storage gate. An optional ion implant is also often used to increase asymmetry. The voltage on ϕ_2 is more positive than on ϕ_1 .

A second method of forming the oxide step consists of growing an initial oxide, selectively etching the oxide in the storage regions, and continuing the oxide growth. Metal is then deposited at an oblique angle so that adjacent gates are electrically isolated as shown in Fig. 2.17 (36,37). In this method, only one metalization and no photoresist patterning is required for metalization.

A third variation of the stepped oxide structure (38,39) is shown in Fig. 2.18. A thick oxide (~ 350 nm) is first grown followed by a thin deposited (~ 100 nm) layer of Al_2O_3 , and a deposited layer of (~ 200 nm) of SiO_2 (to facilitate photolithography). The transfer gates are then defined by selectively etching the Al_2O_3 , the photoresist is removed and the exposed SiO_2 is etched to a thickness of about 100 nm in the storage regions. During this process, the Al_2O_3 over the thick oxide is undercut about 250 nm. About 50 nm of Al_2O_3 is then deposited over the entire structure to seal the gate oxide. Because of this overhang, the metalization (Ti/Pd) is discontinuous as shown. Alternately, a similar overhang can be produced by etching a moat into a thick oxide covered silicon substrate and then regrowing the thin gate oxide (40). The thick oxide overhang produces the metal discontinuity.

A minimum geometry CCD, called the offset gate CCD (41-43) is shown in Fig. 2.19. This structure uses minimum line widths of Si_3N_4 , polysilicon and metal. The Si is first oxidized to protect it from the Si_3N_4 which is then deposited and patterned into strips. Polysilicon is then deposited and patterned to overlap part of the Si_3N_4 . The structure is then oxidized, the unprotected Si_3N_4 is etched away and metal electrodes are deposited.

Another variation of the thin/thick dielectric technique is the VMOS conductively coupled CCD (44) shown in Fig. 2.20. Using anisotropic etching techniques, V's are etched in the Si. The Si is then oxidized, and since the oxide grows fastest at the bottom of the groove, the oxide is thicker here. The conductive coupling between gates is made by ion implantation.

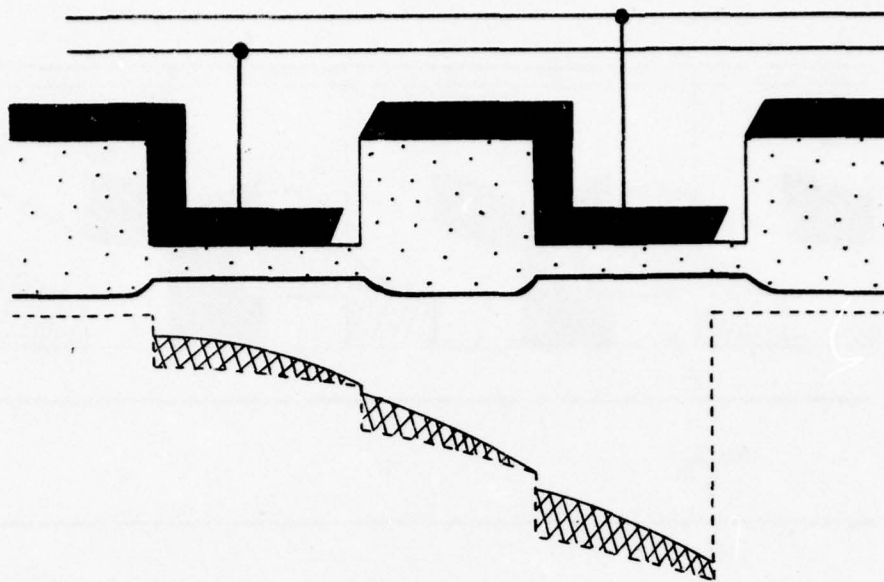


Figure 2.17. Stepped oxide with oblique electrode evaporation

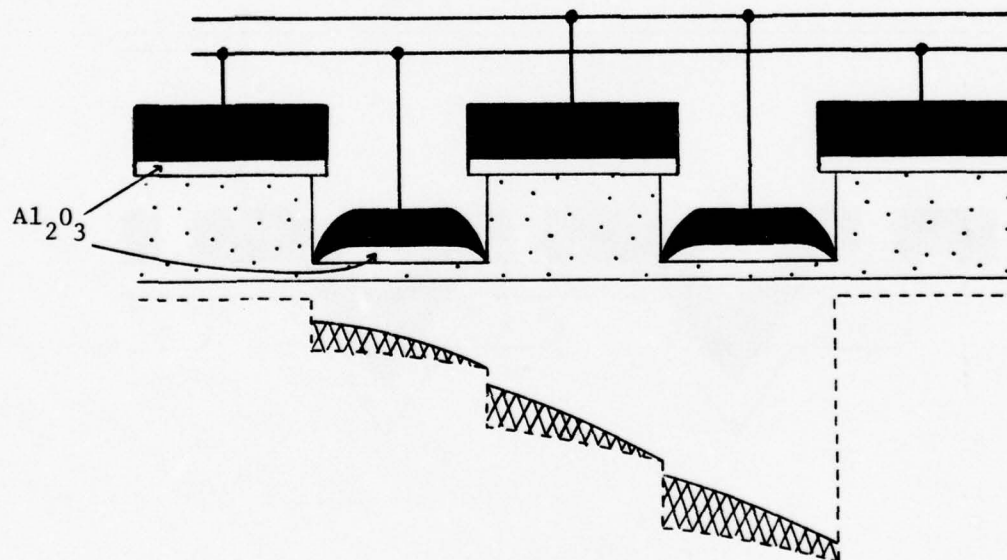


Figure 2.18. Stepped oxide structure using undercutting during etching to eliminate gap problems

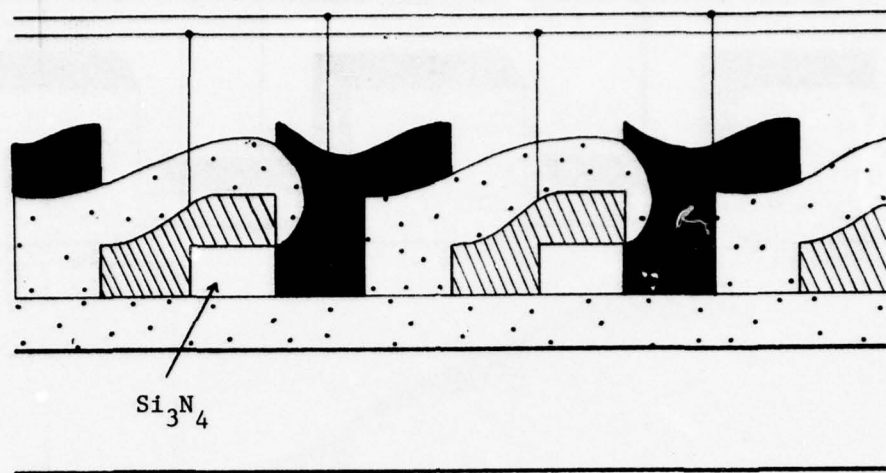


Figure 2.19. Minimum geometry stepped dielectric (offset gate) CCD.

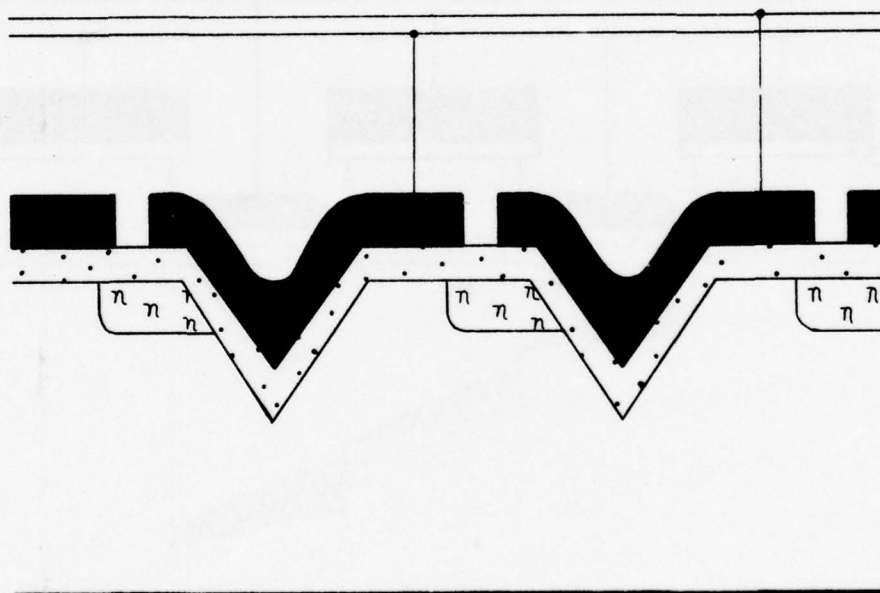


Figure 2.20. V.M.O.S. conductively coupled two-phase CCD.

Ion implantation has been used to create two-phase unidirectional devices (45-48) as shown in Fig. 2.21. P-type ions are implanted near the upstream end of the electrode to increase the net doping there, and thus reducing the depth of the potential well and creating a potential energy barrier. A dose of 1.5×10^{12} boron ions is sufficient to reduce the empty well depth by as much as 7 electron volts in comparison to the nonimplanted region (45). Implanted barriers have advantages over stepped oxide techniques since high potential differences are more easily obtained and the barrier heights are less affected by the applied electrode voltage.

Surface potential can also be modified in MNOS techniques (49) by the presence of immobile charge in trapping centers at the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface or in the Si_3N_4 layer as shown in Fig. 2.22 where positive trapped charge is used with n-type Si substrates.

There are several design considerations for a unidirectional two-phase CCD system. Since part of the electrode is used solely for generating a potential barrier, it is desirable to minimize this length to increase the size and charge handling capabilities of the storage section of the electrode. This length must be large enough, however, to minimize barrier-height depression by fringing field effects. The potential barrier must not extend into the gap region between the electrodes since it would create an uncontrolled barrier that would impede charge transfer. However, if the barrier is located too far from the up-stream edge of the electrode, charge will be trapped behind the barrier (see Fig. 2.22) which gives rise to incomplete charge transfer and noise. Finally, since the barrier height in this system is not as great as the transfer electrode-storage electrode system, an excessive signal charge will be lost over the barrier so that the signal handling is somewhat limited.

A system of conductive connections between electrodes has been devised (47,48,50) which reduces the cell size, relaxes the alignment requirements and avoids gap problems. An n-type ion implant placed between the electrodes forms a conductive bridge through the gaps. The resulting device is known as the conductively connected CCD or C4D. This method can be used with ion

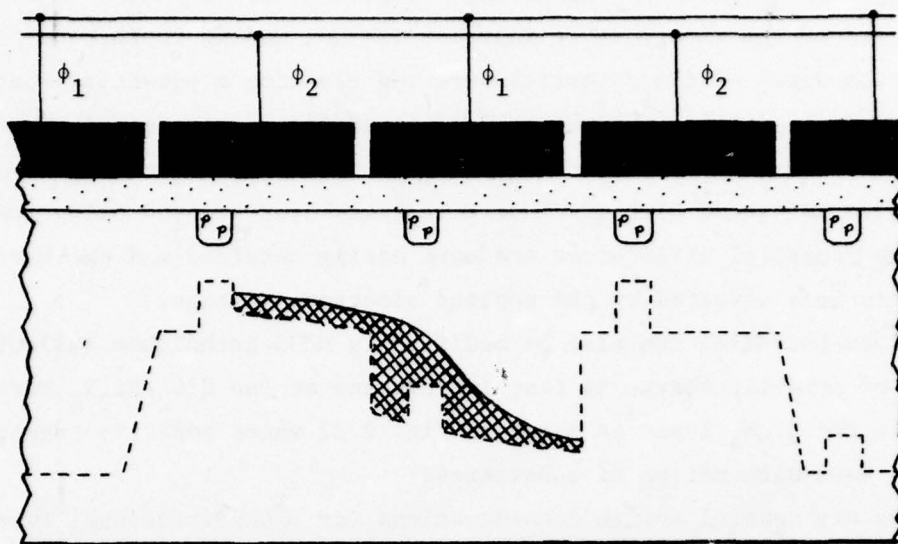


Figure 2.21. Two-phase CCD using localized ion implant to create asymmetry. $V_{\phi_1} > V_{\phi_2}$

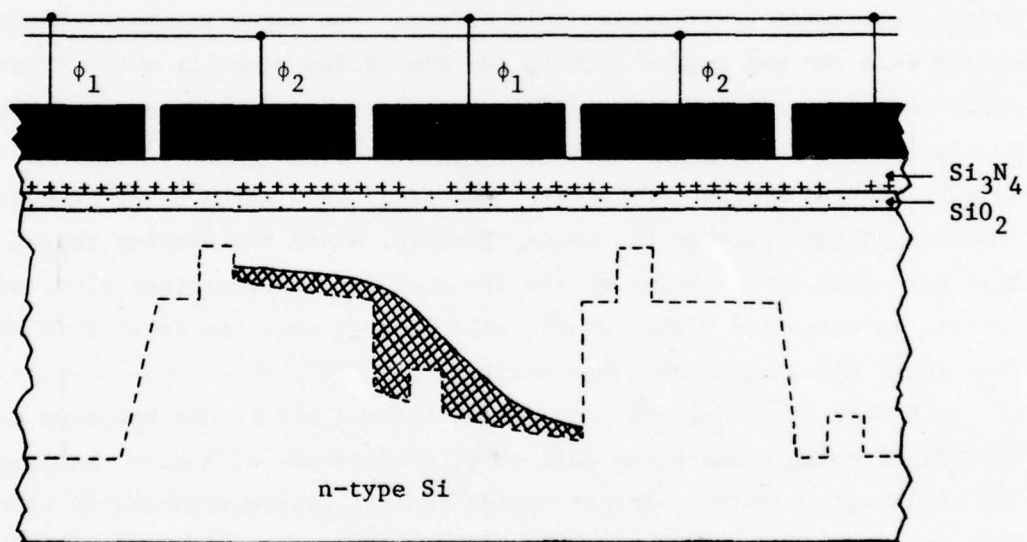


Figure 2.22. Two-phase p-channel CCD using trapped charge in a Si_3N_4 layer to create asymmetry (after 49). $V_{\phi_1} > V_{\phi_2}$

implanted barriers (47) where the restriction on the location of the barrier implant is relaxed since the effects of any barrier implant not covered by the electrode is compensated by the conductive connection implant. This technique has also been used in stepped oxide devices (50).

2.3.3. One-phase systems. Any two-phase system can be operated as a one-phase system if one set of electrodes is connected to a fixed bias and the other set is pulsed positive and negative with respect to this fixed level (51,52). Using combinations of thin/thick oxides and multiple ion implants, systems requiring only single metalizations have been devised (53). MNOS methods can be used to create two accumulation trapping regions which give a three-step surface potential profile (54). While one-phase systems are attractive from an operating standpoint, numerous processing steps are required, and tight tolerances must be kept on ion implants and on MNOS processing and electrode location. Furthermore, signal handling capacity is low. Thus, one-phase CCD's are not in common usage.

2.4. Lateral Confinement

Various electrode structures which produce unidirectional signal charge flow along the oxide-silicon interface or in the bulk have been discussed. However, an important problem concerns the confinement of the signal charge within the channel region so that it is not lost from the lateral edges of the channel. This problem is most severe for n-channel (p-type substrate) devices made on {100} material since this material has a very low interface state density ($\sim 10^9 \text{ cm}^{-2}$). It is less severe for {111} n-type material which has an interface density of 10^{10} - 10^{11} cm^{-3} .

There are three basic methods that are currently utilized to obtain confinement (30).

Thick field oxides (1-2 μm) are commonly used for {111} n-type material where the field threshold voltage can be on the order of 20 volts. This scheme is not satisfactory for CCD's made on {100} Si because to obtain field threshold voltages compatible with normal clock voltages, the oxides required are too thick to permit precise photoresist patterning. Ion implantation is often used to increase the surface impurity concentrations in the field region so that field oxides on the order of 1 μm can be used (see Fig. 2.23a). The ions are implanted just before the field oxidation.

A second approach to lateral channel confinement is the use of a channel stop diffusion as shown in Fig. 2.23b. The channel stop diffusion clamps the surface potential and thus precisely defines the extent of the channel. This diffusion should have about a 10^{19} cm^{-3} surface concentration and should be shallow. Use of a diffused channel stop requires additional masking and process steps but eliminates the need for extremely thick field oxides.

A third approach is the use of an electrostatic field shield as shown in Fig. 2.23c. Normally the field region is covered by a relatively thin field oxide on which a doped polysilicon layer is deposited. The polysilicon is then oxidized and may be covered with other dielectrics. With

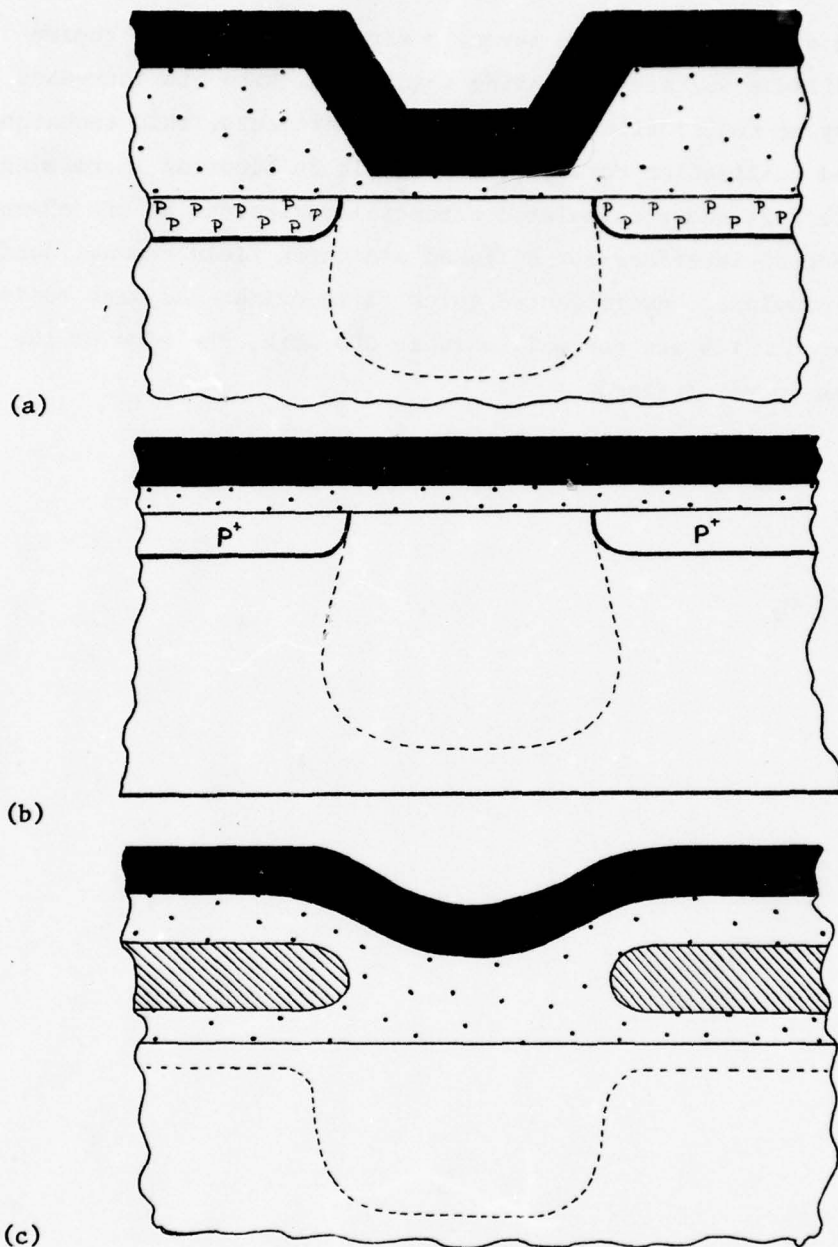


Figure 2.23. Lateral channel confinement techniques. In a, the threshold voltage is increased by use of a thick field oxide outside of the channel region. An additional implant (shown) is optional. In b, a P+ diffused channel stop is used. A polysilicon field shield is shown in c.

proper biasing of the polysilicon layer, a strong accumulation region forms on the silicon surface preventing channeling. With its increased processing, layout restrictions and biasing requirements, this technique has had limited utilization to date, although it is becoming increasingly popular. Figure 2.24 shows calculated potential variations at the channel confinement/channel interface for diffused and thick field channel confinement. For the nonplanar, nonimplanted thick field oxides and high resistivity substrates which are commonly used in CCD work, the edge of the channel becomes poorly defined.

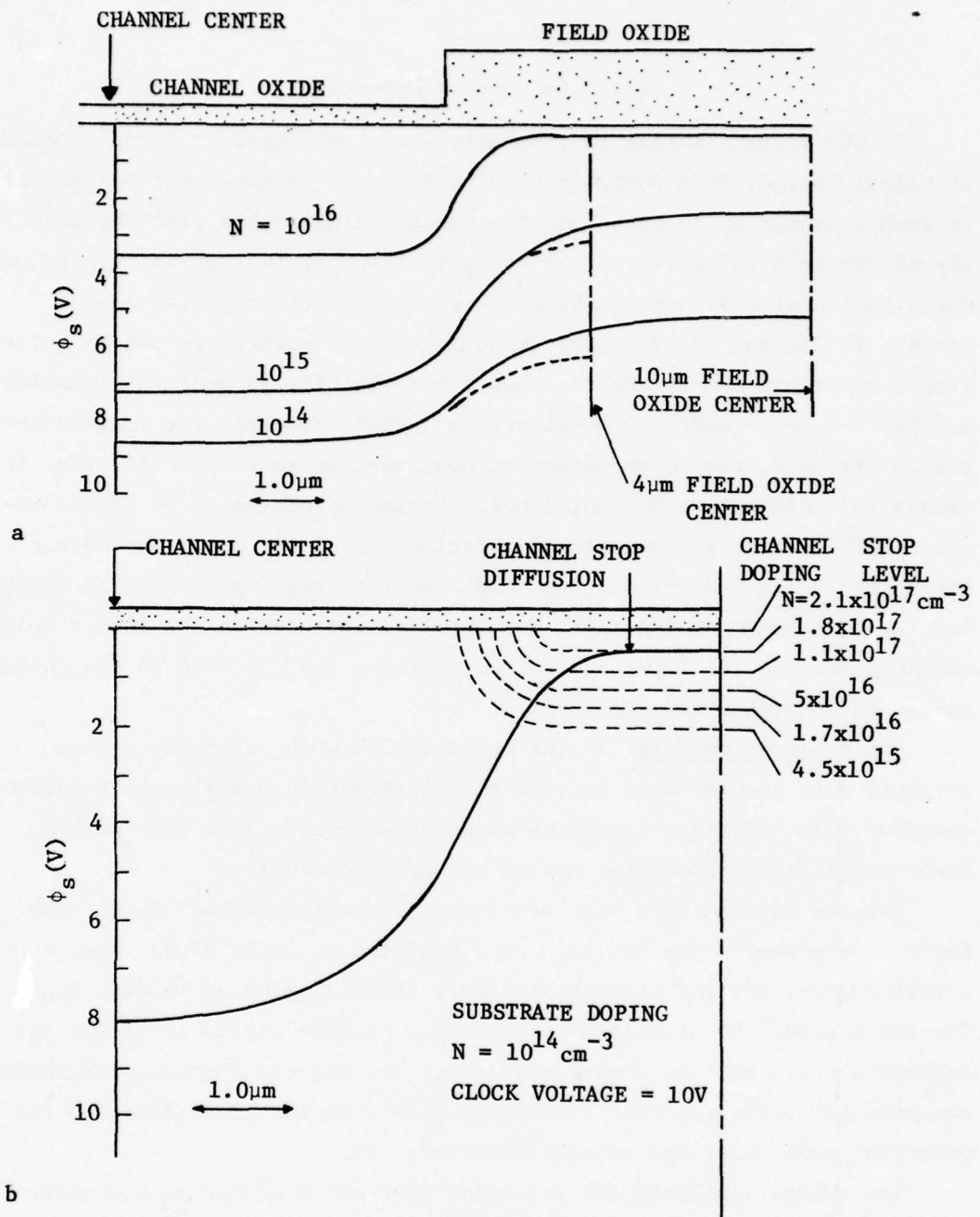


Figure 2.24. Calculated potential profiles for channel confinement techniques: a) non-planar, non-ionimplanted thick field oxide, b) diffusion stop method. Note different scales in a) and b).

2.5. Input-Output Structures

In CCD's, information is transmitted and processed in forms of packets of signal charge. In a useful device, the charge packets must be generated in such a manner as to have some functional relationship with the input signal, whether it be electrical or optical in nature. Similarly, the output signal must bear some functional relationship to the detected charge packet. In digital systems, the input and output structures can be quite simple since any charge greater than a set quantity is generally considered a 'ONE' and less charge is considered a 'ZERO'. However, for imagers and analog circuits, the input-output methods must be very exact in order to retain all information but not generate noise or decrease the signal-to-noise (S/N) ratio. The functional relationship of the input and output circuitry is limited only to the condition that the input function is the inverse of the output function. However, for most devices, a linear relationship between the input and output voltages and the size of the charge packet is desirable for simplicity.

2.5.1. Input methods. In the earliest CCD work, minority charge carriers were generated by driving one electrode into avalanche breakdown and they were collected under the adjacent electrode (5). This method, however, is highly nonlinear and is not used currently.

Various methods have been developed to obtain a linear input. One input arrangement which has been used contains an input diode, one input transfer gate, and one storage electrode (55-57) as shown in Fig. 2.25. The input diode, ID, consists of an n-type surface region in the p-type substrate which acts as a source of electrons for the channel. The input transfer gate, IG, controls the charge flow from the input diode to the potential well under the storage electrode, P2.

The charge available for injection past the transfer gate depends on the signal voltage of the input diode. In Fig. 2.25a the input gate is kept at a constant potential so that the magnitude of the charge packet

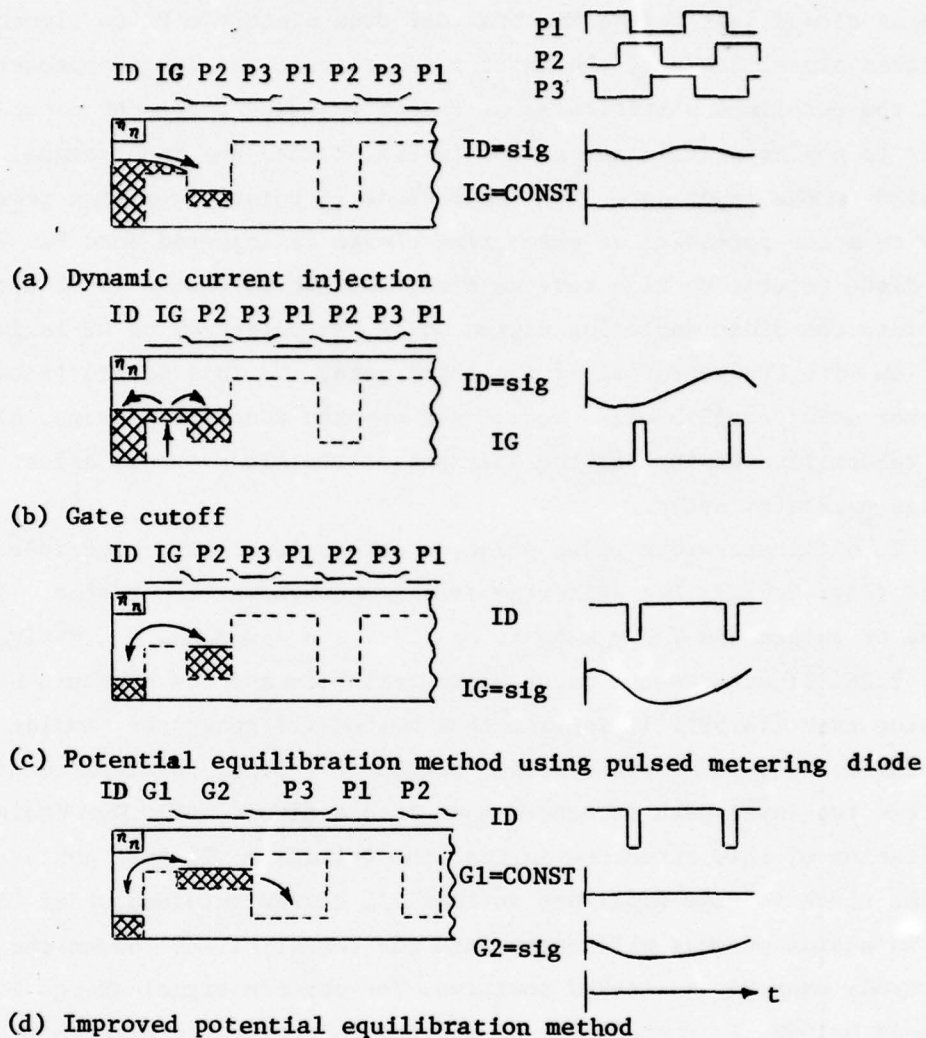
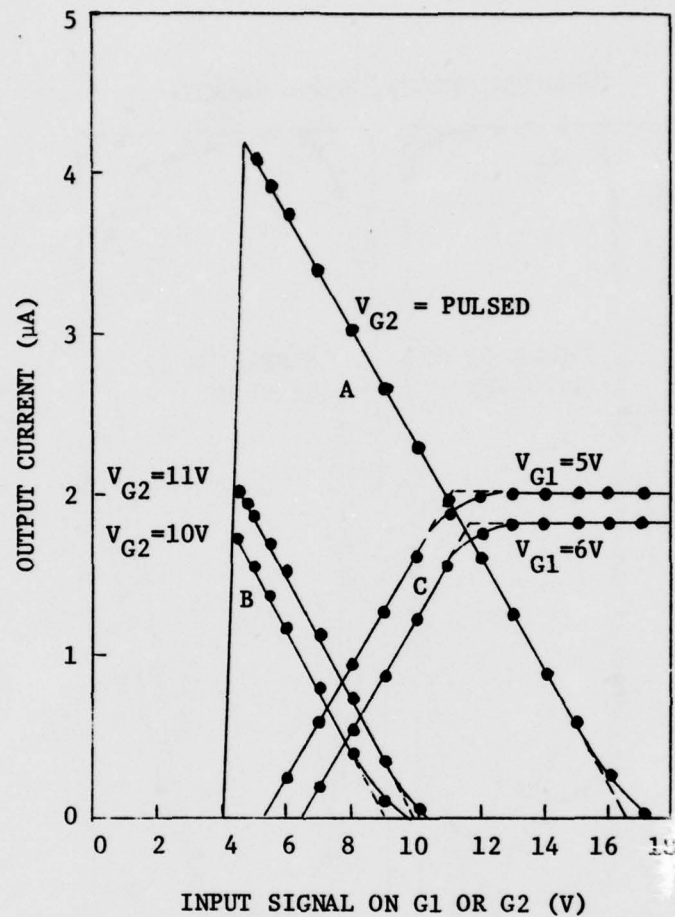


Figure 2.25. Various arrangements for charge injection into a CCD (after 56).

depends on the injection time and on the threshold voltage of the input gate. In Fig. 2.25b, the situation is somewhat improved in that the input gate is closed just before the transfer from electrode P2 to electrode P3 takes place. However, the input gate cannot close instantaneously so that the undefined partitioning of charge residing under the input gate leads to nonlinearities and noise. In Fig. 2.25c, the input signal is applied to the input gate. The input diode is pulsed from high reverse bias to a low potential at which time charge is injected into P2. When the diode returns to high reverse bias, the excess charge in P2 drains off into the diode depletion region until the potential of P2 is in equilibrium with the potential of the input gate, IG. This method is called the potential equilibration method and has had widespread usage, although the random fluctuations of the voltages of the clock pulses affect the charge packet directly.

To eliminate clock pulse noise, a second input gate electrode is introduced (Fig. 2.25d). Two different arrangements have been tested: (1) V_{G2} = fixed or pulsed and V_{G1} = signal, or (2) V_{G1} = fixed and V_{G2} = signal. Fig. 2.26 illustrates the input characteristics and the harmonic content in each case (58,59). It is seen that method (2) generates smaller second and third harmonic components than method (1). Other possible combinations of this two-input gate structure have been analyzed (60). One design limitation of this structure is that the voltage on G2 must not exceed 50% of the clock voltage amplitude so that all charge retained under G2 during the injection process will empty into the potential well under the next electrode when P3 is clocked positive. The maximum signal charge is thus reduced by 50%. To compensate, G2 and the following two electrode areas must be increased by a factor of 2 in order to handle a full sized charge packet. Another variation of this two input gate structure uses feedback to an input of a differential amplifier (61) to achieve linearization.

One problem existing with all described input methods is the sensitivity of device response to variations in threshold voltage. This



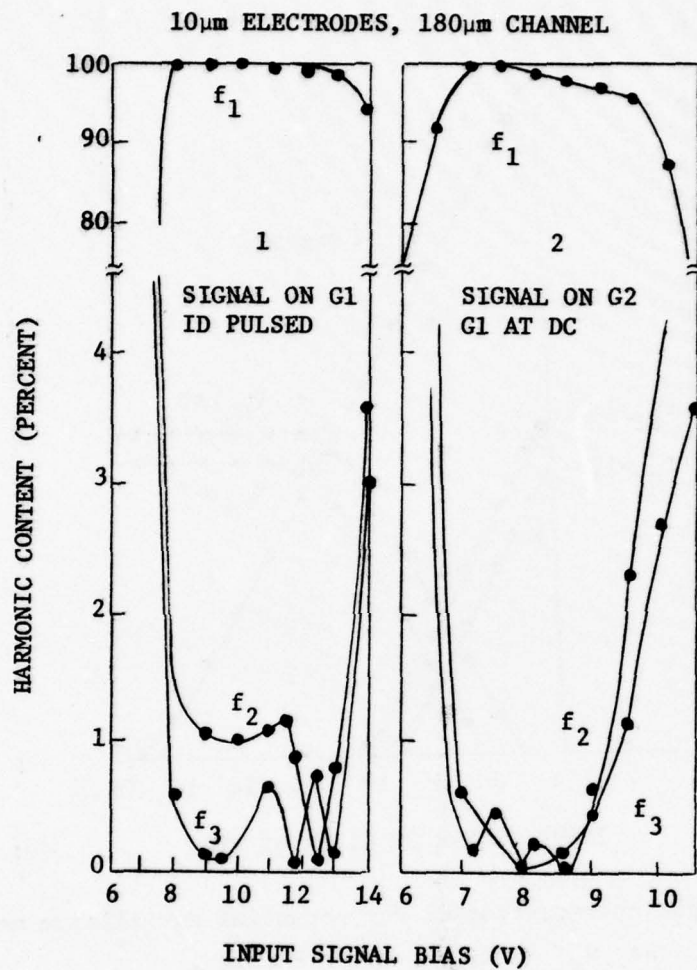
a) Input characteristics for potential equilibrium methods

A: $V_{G1} = \text{Signal}$, $V_{G2} = \text{Pulsed}$

B: $V_{G1} = \text{Signal}$, $V_{G2} = \text{Fixed}$

C: $V_{G1} = \text{Fixed}$, $V_{G2} = \text{Signal}$

Figure 2.26



b) Harmonic content for potential equilibrium input methods of Fig. 2.25(c) and (d) respectively.

Figure 2.26 (cont.) Input characteristics and harmonic content of potential equilibrium input methods (after 56).

sensitivity is caused by slight differences in the threshold voltages of two adjacent electrodes (e.g. G1 and G2 of Fig. 2.25d). Threshold voltages may vary if dielectric thicknesses and processes vary. This is particularly important for multiple inputs which are physically separated from each other. One method (62) which reduces the threshold voltage sensitivity also controls the injected charge by sequential application of different voltage levels to the same electrode. Fig. 2.27 illustrates the basic concept. The signal voltage, V_{sig} , is first applied to the gate of T_1 allowing excess charge to flow into the region of the floating diffusion such that the charge is equal to $(V_{sig} - V_T)C'_{FD}$, when V_T is the threshold voltage of T_1 and C'_{FD} is the capacitance of the floating diffusion. The input gate is then opened and V_{ref} is applied to the gate of T_1 . Charge flows into the CCD until the voltage on C'_{FD} has risen to $V_{ref} - V_T$. Thus,

$$Q'_{in} = (V_{ref} - V_T)C'_{FD} - (V_{sig} - V_T)C'_{FD}$$

or

$$Q'_{in} = (V_{ref} - V_{sig})C'_{FD}$$

On a 10 input multiplexer circuit, the fixed pattern noise was reported to be reduced by an order of magnitude by the use of this scheme.

2.5.2. Detection methods. There are three basic methods of charge detection which have been used extensively. In an early CCD demonstration (5), the electrode containing the charge packet was biased into accumulation and the charge was dumped into the substrate. Substrate current was then sensed as the output signal. This method, however, permits only one packet to be dumped at a time. In addition, the time between dumps depends on the recombination rate. Large CID imagers (63) have employed this method using epitaxial material for the active region and with reverse bias on the substrate junction to increase the recombination rate.

The second detection method employs an output diode. The diode is biased more positively than the maximum surface potential located under

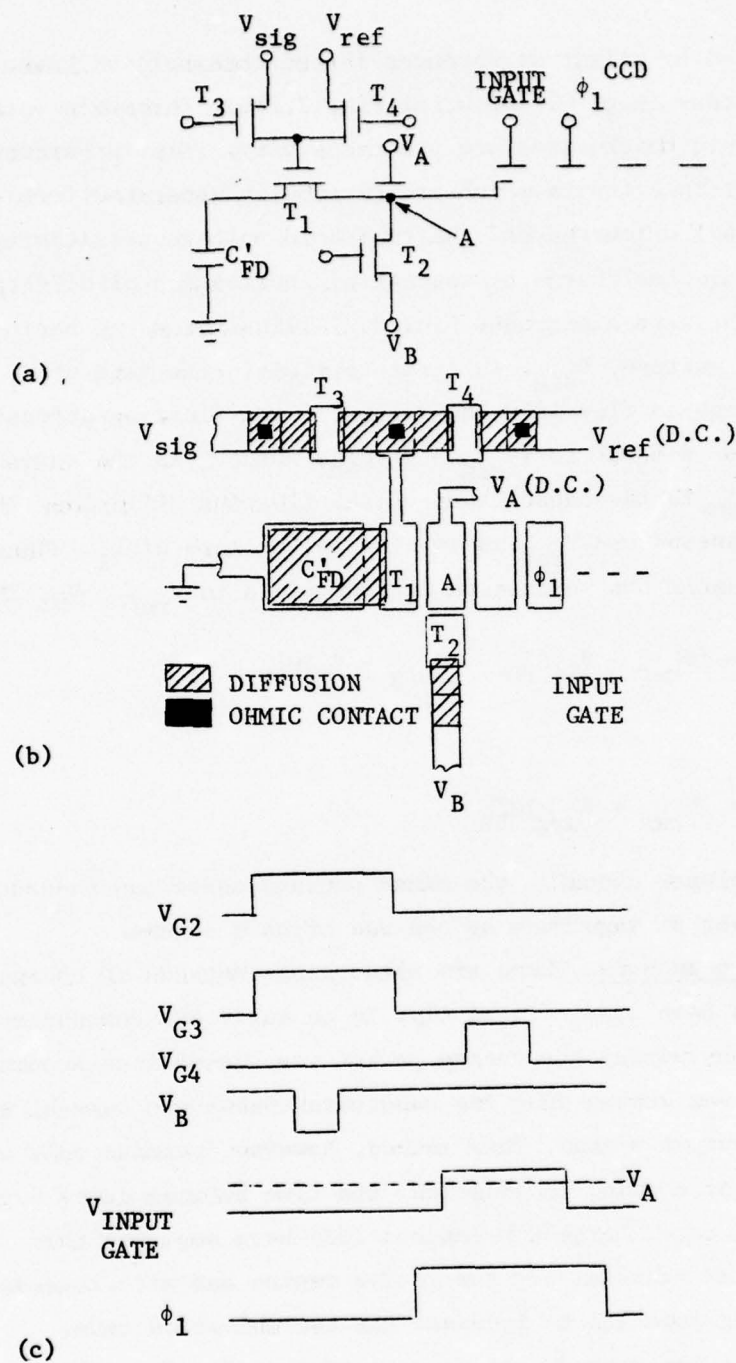


Figure 2.27. Input circuit with reduced threshold voltage sensitivity: a) schematic diagram, b) circuit layout and c) operating waveforms (after 62).

the last (or output) electrode so that the signal charge will be dumped into the depletion region of the diode. Initially, various off-chip detector amplifier circuits were used. In one, the output diode was connected to a constant voltage source via a $1\text{ M}\Omega$ resistor with a gated integrator to record the current flow (64). This elementary system was improved by using current feedback on a current sensitive preamplifier thus creating a low impedance input. The voltage on the diode thus remains relatively constant. By using a low pass filter to eliminate noise and harmonics of the signal, good linearity can be achieved with this system.

To eliminate losses and parasitic capacitances, on-chip MOSFET sense amplifiers and reset circuitry have been developed (30-32,65) as shown in Fig. 2.28. In this case, the detector is a diffused region under G-3 which is connected to the gate of a MOSFET amplifier. During the ϕ -2 cycle, this diffused region is reset to the voltage on D-1 by gating G-4 on and then is electrically isolated by gating G-4 off. The signal charge is then dropped into the floating diffusion region during the ϕ -1 cycle. The resultant potential of this floating diffusion is transferred to the gate of a MOSFET where it is amplified. Output voltages of up to 10 volts and frequency response up to 10 MHz have been reported using this device. Another way of sensing the signal using this structure is to monitor the voltage of electrode G-3 each time it contains the signal charge packet.

These detection systems are susceptible to noise during the reset cycle. A correlated double sampling system (66,67) has been developed to eliminate this reset noise.

A third detection system uses a floating gate above the channel which senses the size of the charge packet by its image charge on the gate (8,28,68-74). When the charge packet is transferred to the well under the floating gate, the potential on the floating gate decreases as

$$\Delta V_{FG} = \frac{\Delta Q'}{C_{FG}}$$

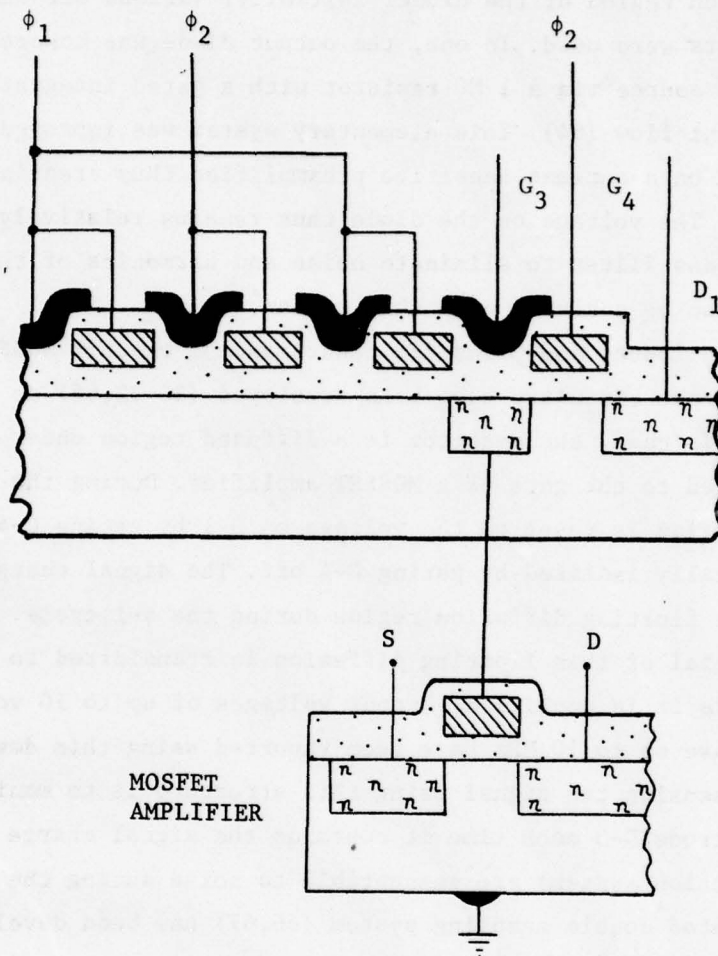


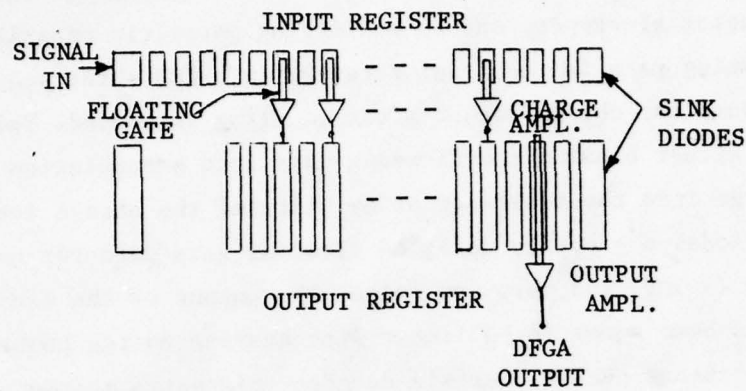
Figure 2.28. Signal detector and output amplifier (on-chip).

To maximize the output voltage of the floating gate, the capacitance must be minimized. This is done by minimizing its area consistent with adequate charge handling capability, using as large a substrate resistivity as permitted by other considerations, using a thick oxide between the floating gate and the biasing electrode, and by minimizing parasitic capacitance.

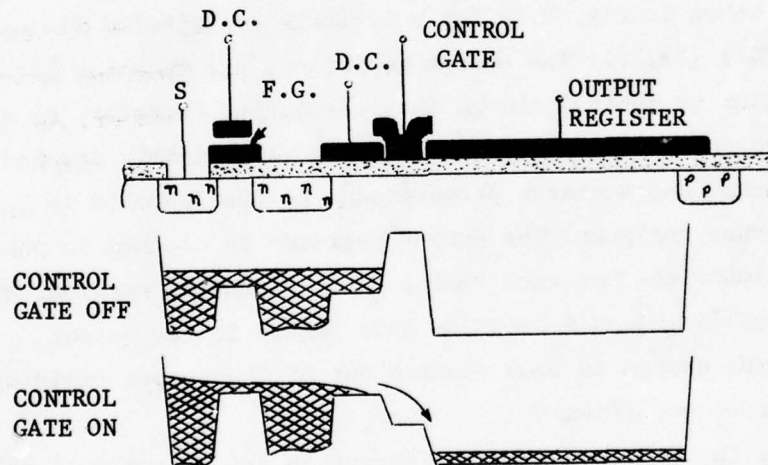
If the floating gate is the final detector in a CCD shift register, some method to dump the charge packet after sampling is needed. This is accomplished by either biasing the floating gate into accumulation and dumping the charge into the substrate or by shifting the charge into a reverse biased diode. A properly designed floating gate detector has very high sensitivity ($\sim 5\mu\text{V}$) and very low noise. The output of the floating gate detector has been shown to be linear with respect to the number of electrons in the charge packet over six decades. Since the charge packets under the floating gate are not disturbed while being monitored, it is possible to read the charge packets several times as they pass down a register. This is shown in Fig. 2.29 for a 12-stage distributed floating gate amplifier (DFGA) (72,75). The charge amplifiers use floating gates on the input register to control charge into the output register. As a signal charge moves down the input register it is periodically sampled by the charge amplifiers, and a charge proportional to that sampled is injected into the output register. The output register is clocked in phase with the input register so that each time a given packet is sampled, the corresponding charge is injected into the same packet in the output register*. The output charge is then clocked out of the output register by a floating gate output amplifier.

Theoretically, the S/N ratio should improve as the square root of the number of stages of the DFGA. The rms noise has been measured at approximately 10-20 electrons with a bandwidth of 3 MHz. The minimum acceptable

* Actually, the charge amplifiers act as inverters.



(a) Schematic Diagram



(b) Charge Amplifier Operation

Figure 2.29. Twelve-Stage floating gate amplifier (after 72).

detectable input signal is approximately 300 electrons and saturates at about 10^5 electrons. Thus, for small charge packets, such as imagers, this amplifier can improve the dynamic range and minimize noise in charge detection.

2.6. Regeneration Systems

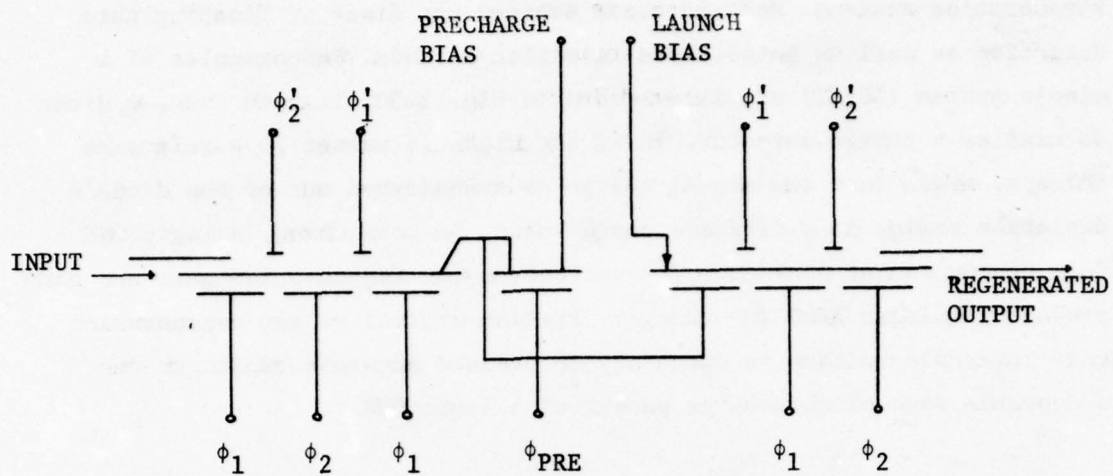
Ideally, one would like to use long arrays of CCD's for memory, and other applications without the use of additional circuitry. But, because of transfer inefficiency and dark currents (discussed in Chapter 3), the information contained in each charge packet degrades as it moves through the CCD. Thus, after a certain number of transfers and/or time has elapsed, it is necessary to refresh or regenerate the charge packet to its original state.

The number of complete cell transfers attainable depends inversely on the number of transfers required per cell. This consideration forms an upper bound on the number of cells between regeneration circuits. The electrons thermally generated in the register, or dark current, create noise. The noise is then increased as the time between regeneration increases. As a result, the number of cells permitted between regeneration circuits varies directly with the operating or clock frequency.

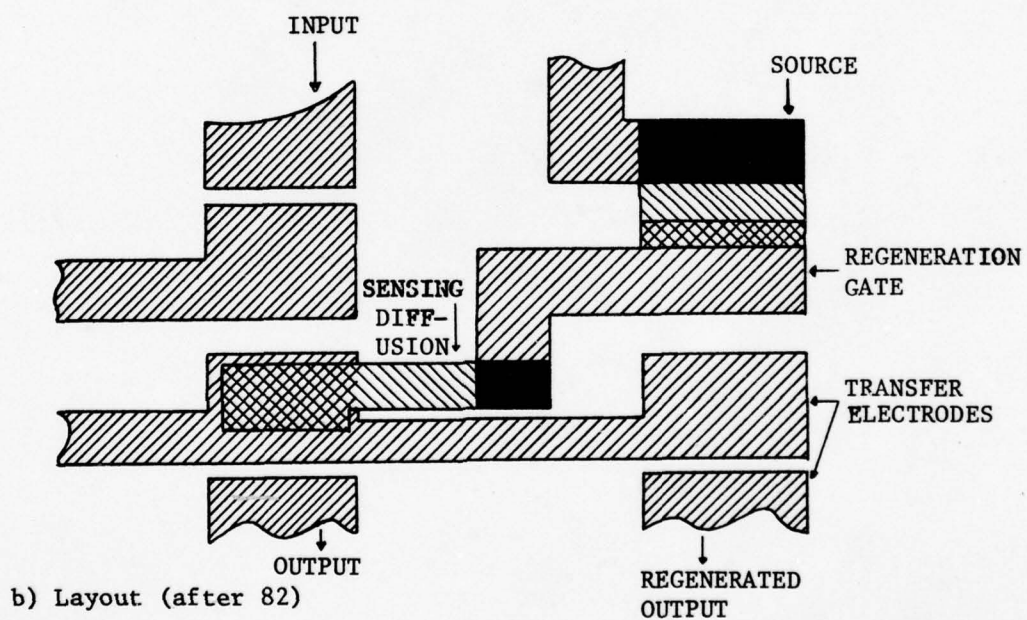
The requirements for regeneration circuits are not particularly severe for digital CCD's where only the presence of a zero or a one need be detected and regenerated. Analog CCD's, and multilevel digital CCD's, however, require good linearity and stability in the regeneration circuits. To date, little work has been done on the development of analog regeneration circuits. Fortunately, many analog circuits such as delay lines, correlators, and transversal filters, can be designed with relatively few (less than 300) stages and do not require signal regeneration. In imagers, some work has been done in recirculation of the charge through the image repeatedly to minimize dark current pattern noise and to detect motion (76). Experimentation on the measurement of transfer efficiency is underway via multiple recirculation of a pulse train through a 200 stage shift register (77).

There has been considerable development of digital regeneration systems (29,48,68,78-82). Various methods of charge detection and injection have been combined to form a variety of inverting or non-inverting binary

regeneration systems. Most of these systems use diode or floating gate detection as well as gated diode injection methods. Two examples of a simple system (80,82) are illustrated in Fig. 2.30. In each case, a diode is used as a charge detector. In a, the diode is preset to a reference voltage, while in b the signal charge is transferred out of the diode's depletion region to a diffused charge sink. In both cases, a logic ONE full charge packet decreases the voltage on the regeneration gate and thus producing a logic ZERO (no charge). Precise control of the regeneration gate threshold voltage is necessary to produce accurate limits on the acceptable size of the charge packet of a logic ONE.



a) Schematic diagram (after 80)



b) Layout (after 82)

Figure 2.30. Digital regeneration systems.

2.7. Review of Basic CCD Processing

In many respects the processing of MOS devices and CCD's are similar. First, both use similar starting material except that for the CCD, the minority carrier lifetime is longer, and thus the generation rate and the dark current are reduced, and the resistivity is higher (10-40 ohm-cm for n-channel CCD's, vs 5-10 ohm-cm for p-channel CCD's). Second, the basic processing steps, oxidation, diffusion, ion implantation, metalization, etc. are similar in principle.

In the fabrication of early CCD's, basic MOS technology was used. However, as CCD technology matured, significant differences and refinement of the basic MOS process occurred. CCD technology is more demanding of the material and of the process control than is MOS technology. From basic CCD process descriptions, only a few obvious process changes from MOS processing (83,84) are detected although some changes have been made in the MOS design rules for application to CCD layouts.

As indicated earlier, dark current is a major restriction on the number of stages in a CCD without regeneration. Dark current results from the thermal excitation of electrons from the Si valence band into the conduction band via interband defect states within the Si bulk (bulk states) or at the SiO_2/Si interface (interface states). To minimize dark current it is necessary to minimize the density of these states.

It has been found that processing above 1100°C and rapid cooling of the Si wafers contributes to bulk states. Presently, temperatures above 1100°C are not used, and the wafers are cooled at a low rate, either by removing them slowly from the furnace or by slowly lowering the furnace temperature. To minimize lattice defects near the front surfaces in the first processing step, the wafers are often stressed on the wafer backside by heavy ion implantation or heavy phosphorus diffusion. The backside then acts as a sink for lattice defects. Phosphorus gettering is used to remove iron, copper and gold precipitates from lattice defect sites.

Annealing at low ($\sim 400^\circ\text{C}$) and high (800-900°C) temperatures is also commonly used to decrease bulk and surface carrier generation time and thus reduce dark current.

Because minority carrier generation in the gate regions contributes to dark current, the interface state density must be low in these regions. The interface state density must also be uniform across the wafer and be reproducible because of the tight tolerances on the threshold voltages. Thus the gate oxidation is a critical step in CCD's. Oxidations involving HCl have been shown to decrease generation rates significantly (83) and are generally used (except for some field oxidations where the quality is of less importance and the speed of wet oxidation is desired).

In some cases, as for CCD's using triple polysilicon gate levels, the gate oxide may have to be grown more than once with a resultant increase in the interface state density. Although the procedure for minimizing interface states is reasonably well understood for single oxidations and nitrogen anneals, it is not well defined for multiple oxidations. As a result, combination gate dielectrics are becoming more popular. $\text{Si}_3\text{N}_4/\text{SiO}_2$ and $\text{Al}_2\text{O}_3/\text{SiO}_2$ combinations as gate dielectrics necessitate only one gate oxidation since the Si_3N_4 or Al_2O_3 layer protects the SiO_2 from subsequent etchings.

Other areas are changing because of CCD processing specifications. Overlapping polysilicon levels which require pinhole-free thermal oxidation, and in some cases, deposited oxides or nitrides to achieve good isolation between gates are becoming common. The amount of polysilicon used on a chip is increasing significantly and polysilicon patterning tolerances are becoming more stringent as packing density increases. For bulk CCD's, the epitaxial layers on ion implanted regions must have their impurity concentrations accurately controlled.

As is the case for MOS device fabrication, numerous variations of the basic processing methods are used. One possible example of the fabrication of a typical n-channel, planar, double level overlapping polysilicon, two component gate dielectric surface channel CCD is outlined below. Since this procedure involves a combination of various processes which depend in part on the experience of the manufacturer, it is improbable that any

manufacturer follows the precise procedure, but it serves to illustrate the various process sets.

The steps are as follows:

1. Selection of wafers: p-type, {100}, 10-30 ohm-cm. Optional: various "gettering" steps on backside of wafer such as implants, mechanical stressing, diffusion, etc.
2. Oxidization of wafers
3. Deposition of $\text{Si}_3\text{N}_4/\text{SiO}_2$
4. Field oxide photoresist
5. Etching of $\text{SiO}_2/\text{Si}_3\text{N}_4$
6. Field threshold boron implant
7. Field oxidation
8. Etching of $\text{SiO}_2/\text{Si}_3\text{N}_4$ from device region
9. Bulk channel phosphorus implant
10. Etching of SiO_2
11. Gate oxidation
12. Deposition of gate Si_3N_4
13. Deposition of polysilicon. Optional: Threshold voltage implant in NMOS control circuitry
14. Phosphorus diffusion
15. Oxidation, photoresist and etching of polysilicon
16. Channel barrier implant
17. Deposition of polysilicon
18. Phosphorus diffusion
19. Oxidation, photoresist and etching of polysilicon
20. Oxidation of polysilicon
21. Photoresist of drain/source regions, etc.
22. Phosphorus implant or diffusion
23. Photoresist and etching of contact holes
24. Deposition of aluminum
25. Photoresist metalization

- 26. Etching of metalization
- 27. Deposition of overglass
- 28. Photoresist and etching of overglass
- 29. Anneal metalization

If diffused channel stops (rails) are required, an additional photoresist and phosphorus diffusion step is required between Steps 8 and 9.

As can be seen, a typical n-channel, CCD process is not as simple as initially envisioned. Of course, each step and the sequence of steps could be changed in numerous ways to fit each manufacturer's process requirement, and equipment restrictions.

2.8. Future Trends in Processing

The trends in CCD processing are not entirely clear because manufacturers do not make a policy of publishing detailed processing information. But, it is clear that a significant effort is currently being undertaken to improve the quality of the wafers through various gettering steps (ion implantation, diffusion, abrasion, epitaxy, etc.), to decrease the dark currents and to increase uniformity. Bulk channel devices, particularly versions of the profiled peristaltic device, seem to be growing in popularity, and will probably continue to do so if the dark current problem can be solved. Compound gate dielectric structures ($\text{SiO}_2/\text{Si}_3\text{N}_4$, $\text{SiO}_2/\text{Al}_2\text{O}_3$, etc.) are becoming more widespread because of significant process simplifications which have removed undesirable steps. Polysilicon will continue to be used as electrodes, with some work being done to decrease the polysilicon resistivity. Numerous metalizations have been investigated but aluminum or an aluminum alloy (Al-Si, Al-Cu, etc.) will probably be used exclusively in production devices. Ion implantation is rapidly replacing all diffusion steps, except possibly the polysilicon diffusion steps. In addition, it is probable that ion implanted planar field oxidation will replace polysilicon shields, except in special applications.

2.9. Design Rules

In a rapidly developing technology such as the CCD technology, design rules for chip layouts which are currently employed in industry are difficult to define accurately. However, the CCD design rules have been generated from standard MOS design rules and thus are similar. In addition, most CCD circuits have on-chip MOS control circuitry, such as shift registers, input/output circuits, sense amplifiers, refresh amplifiers, etc., which are designed according to only slightly modified MOS design rules. These modifications in the structure and processing of CCD's as compared to MOS devices are sufficiently different so as to warrant the development of new design rules. Among process and design variations, typical CCD structures include two levels of polysilicon electrodes, diffused or implanted channel stop rails, field threshold control ion implants and barrier ion implants. Due to the increased packing density of CCD elements, the standard MOS design rules have been adopted to minimize size whenever possible.

The following dimensions are typical design rules for CCD layouts which are currently in use in the industry.

Polysilicon line width:	5 μm min
Space between polysilicon lines	5 μm min
Top polysilicon line overlap with lower polysilicon line	1 μm min
Channel stop width - diffused	6 μm min
" " " - implanted	4 μm min
Ion implanted barrier width	4 μm min
Contact holes to polysilicon	5 μm x 5 μm min
Width of thin oxide for stepped oxide configuration	6 μm min
Width of thick oxide for stepped oxide configuration	4 μm min
Aluminum line width	7 μm min
Aluminum line spacing	7 μm min

These dimensions are typical in industry and exhibit the current trends. Numerous additional design rules are certainly required to form a complete set, but the above rules illustrate the main points of current thinking in the industry. Process and equipment improvements which are currently under investigation should significantly decrease these dimensions in the near future. Electron beam and similar exposure methods should eliminate the lithographic process limitations to minimum feature dimensions. Process variation, such as offset masking, oblique metal deposition, etc., will offer additional help in minimizing the process-related limitations in the design rules. After the process limitations have been reduced, the effects of scaling will be considered because doping concentrations

and depth dimensions such as depletion widths, oxide thicknesses, operating voltages, etc. must be scaled together in order to maintain a properly functioning design. As the charge storage area decreases, the total signal charge decreases and thus improved on-chip detection systems will be required.

In Table 2.1, a comparison of the minimized cell size is shown for 2-phase offset, standard 2-phase, 3-phase and 2 level, and 3-phase and 3-level CCD structures. In this table, C is the photolithographic size of one phase of the CCD cell, and R is the normal registration tolerance. From a circuit design standpoint, L_{st} is the minimum desirable storage well length and L_{tr} is the minimum desirable transfer gate length.

Structure	Photolitho- graphy Limita- tions	Design Limita- tions	Current minimum Cell * Length	Future Minimum Cell * Length	Mask Lead
2-phase offset	2C	$2(L_{st} + L_{tr} + 2R)$	20 μ m	12 μ m	3
Standard 2-phase	4C+4R	$2(L_{st} + L_{tr})$	32 μ m	12 μ m	2
3-phase 2-level	3(C+2R)	$3L_{st}$	30 μ m	12 μ m	2
3-phase 3-level	3C	$3(L_{st} + R)$	18 μ m	9 μ m	3

* Calculations involved design rules.

Current

$$C = 6\mu\text{m}$$

$$R = 2\mu\text{m}$$

$$L_{st} = 4\mu\text{m}$$

$$L_{tr} = 2\mu\text{m}$$

Future

$$C = 2\mu\text{m}$$

$$R = 1\mu\text{m}$$

$$L_{st} = 2\mu\text{m}$$

$$L_{tr} = 2\mu\text{m}$$

TABLE 2.1. Minimum Cell Length Comparison (after 74).

3. CCD CAPABILITIES AND LIMITATIONS

The CCD is inherently a simple device. As a result, its various configurations are relatively easy to analyze, and many theoretical studies have been published relating the physical properties of a CCD to its electrical characteristics. Of particular interest are signal handling capabilities, transfer efficiencies, noise, and power dissipation. These parameters are related to such device characteristics as signal-to-noise (S/N) ratio, frequency response, input/output signals, clock voltage waveforms and magnitudes, etc.

3.1. Signal Handling Capabilities

In CCD circuits, especially those used for signal processing, the signal handling capability is of major importance. Although large signals improve the S/N ratio, they also require large electrodes which increase the circuit size, and larger clock voltages which increase power dissipation. A trade-off is required. The methods used to optimize signal handling capabilities are different for SCCD's than for BCCD's.

3.1.1. Signal handling capabilities of SCCD's. The maximum charge that can be accommodated in a SCCD without spilling over into the substrate is given by Eq. 2.11, ($Q_{n \max} = -C_{ox} V_G$), and is proportional to V_G . However, excessive values of V_G can cause breakdown. In an empty well, V_G is dropped mainly in the Si and avalanche breakdown can occur for large V_G . For a full well, V_G is dropped primarily across the oxide and dielectric breakdown can occur. The latter condition usually limits the maximum value of V_G . Considering that the breakdown field ϵ_{\max} in SiO_2 is $1-5 \times 10^6$ V/cm,

$$Q_{n \max} = \epsilon_{ox} \epsilon_{\max} \sim 2 \times 10^{12} - 1 \times 10^{13} \text{ electrons/cm}^2 \quad (3.1)$$

In compound dielectric structures, such as Si_3N_4/SiO_2 or Al_2O_3/SiO_2 , $Q_{n \max}$ can be somewhat larger.

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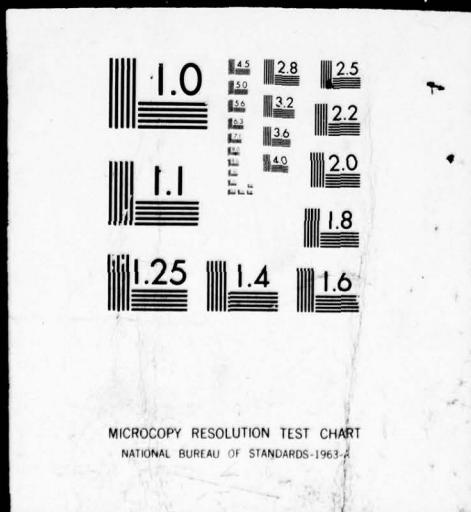
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In normal operation, a CCD is biased so that all electrodes are above the threshold voltage in order to avoid charge pumping^{*} (7,85). This condition can be achieved by biasing all electrodes with a voltage greater than the threshold voltage, V_T , or by applying a negative bias to the substrate. In a normal CCD, the electrodes are electrically connected so that no uncontrolled surface potential barriers occur between electrodes. The maximum signal charge is, then, a function of the potential difference between adjacent potential wells. If additional signal charge is added, the excess charge will flow away from the full well into other potential wells and redistribute itself until potential equilibrium is achieved, rather than being injected into the substrate. Assuming that the adjacent electrodes are held at a low voltage, V_L , the signal charge per unit area that can be held under an electrode biased at the high voltage, V_H , is approximated from Eq. 2.11,

$$Q_n \approx -(V_H - V_L)C_{ox} = -(V_H - V_L) \frac{\epsilon_{ox}}{d_{ox}} \quad (3.2a)$$

For $(V_H - V_L) = 10$ V and $d_{ox} = 100$ nm, Q_n is 3.4×10^7 C/cm² which corresponds to 2.1×10^{12} electrons/cm². It is noted that this value is close to that which results in dielectric breakdown of the SiO₂.

Letting Q'_n represent the total charge in the potential well, Eq. 3.2a becomes

$$Q'_n \approx -(V_H - V_L)C_{ox}WL = -(V_H - V_L) \frac{\epsilon_{ox}WL}{d_{ox}} \quad (3.2b)$$

where the gate width and length are represented by W and L respectively.

For three-phase devices, the maximum signal current $I_{s3\phi}$ for a voltage pulse magnitude $V_p = V_H - V_L$ can be determined as

$$I_{s3\phi} = Q'_n f_c = V_p W L C_{ox} f_c \quad (3.3)$$

where f_c is the clock frequency. For the previous example, if $W = 20$ μ m, $L = 10$ μ m and $f_c = 1$ MHz, then

$$Q'_n = 4.3 \times 10^6 \text{ electrons or } 0.69 \text{ pC}$$

* Charge pumping involves injection of charge from the channel into the substrate upon removal of the "high" gate voltage.

and

$$I_{s_{3\phi}} = 0.69 \mu A$$

Clock waveforms and the relative time relationship between the three clocks are important in three-phase systems. The potential field of the sending electrode should not collapse before the potential well of the receiving electrode is established, or the excess charge will be dumped into the substrate. Thus, the two clock waveforms must overlap as shown in Figure 3.1a. The maximum charge handling capability exists for rectangular clock pulses. If the waveforms are changed such that only two clocks are used in an asymmetrical 2-phase fashion with the third phase held at an optimum immediate value, the expected charge handling reduction is 50% but was found experimentally to be 40% of that for square pulse operation (86). For sine wave clock drive, the capacity is reduced to approximately 75% of that for square waves because of the decrease in the relative potential difference between adjacent electrodes. The charge handling capacity for these schemes is shown in Fig. 3.2.

Four-phase devices theoretically should have the same charge handling capabilities as similar size three-phase devices if they are clocked as shown in Fig. 3.1b. However, since four-phase devices have an extra electrode, it is possible to combine two adjacent electrodes into one storage electrode and effectively double the charge handling capability of the device (Fig. 3.1c). Similarly, it is also possible to use the two adjacent electrodes of a 3-phase device as storage electrodes to increase the charge handling capabilities of three-phase imagers (87).

Two-phase devices using four-phase clocks have the same charge handling capabilities as three-phase devices. However, for two-phase devices using potential barriers formed by stepped oxide or ion implantation, the barrier potential is fixed by the process and limits the charge handling capabilities. Since process generated potential barriers are not as great as those generated by the application of two different voltages, the two-phase CCD can be expected to have somewhat less charge handling capability

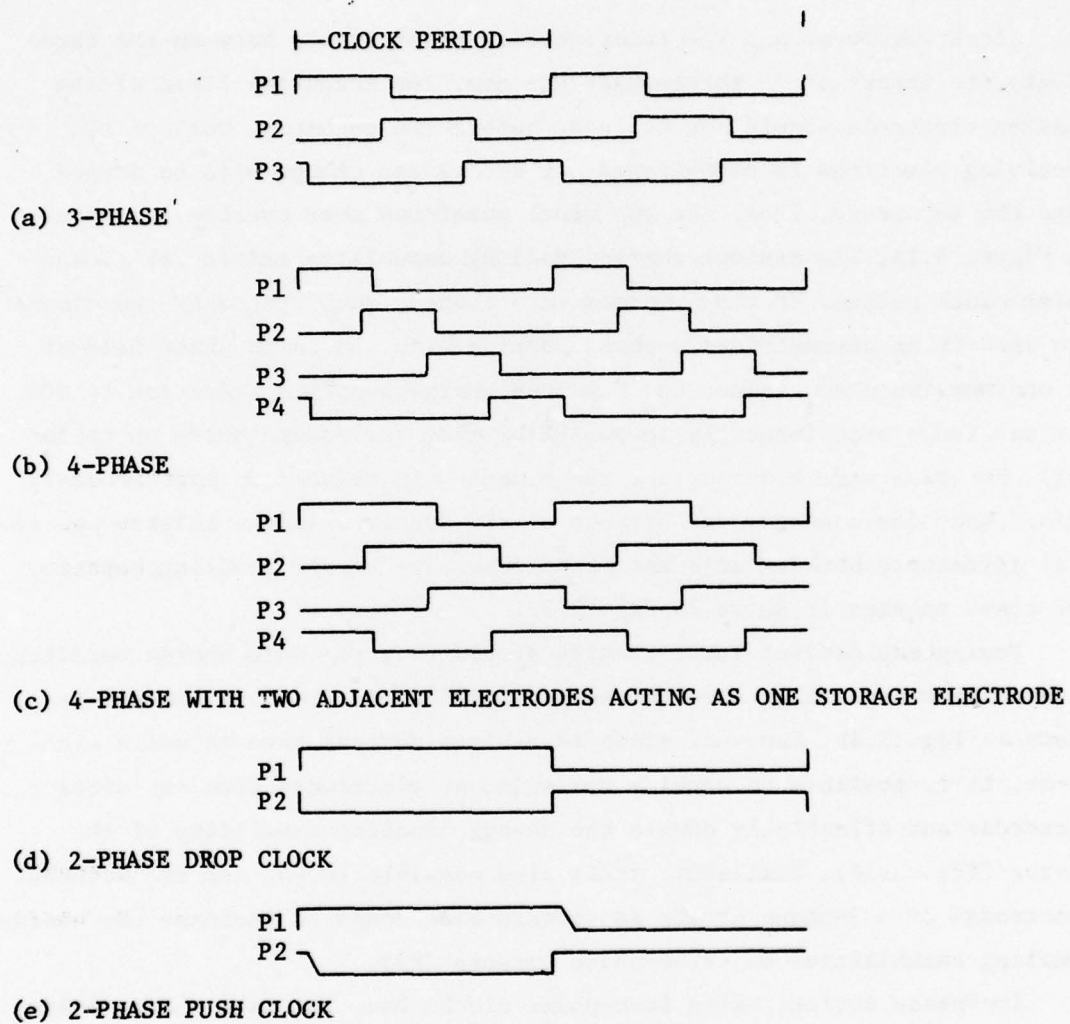


Figure 3.1. Operating pulse waveforms for various CCD's. Note phase overlap in (a), (b), (c), and (e). (After 9).

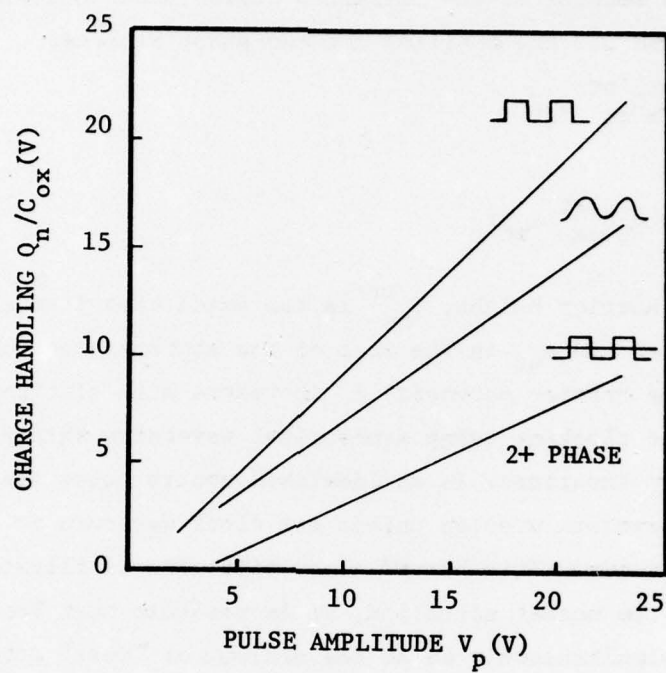


Figure 3.2. Maximum charge handling capacity of SCCD for various 3-phase square and sinusoidal waveforms and for 2+phase asymmetrical waveform (after 86).

than those of three-phase and four electrode two-phase CCD's. Figure 3.3 indicates the potential barriers which can be produced with stepped oxide and with ion implantation techniques. In the case of the ion-implanted barrier, the effective electrode size is significantly smaller than the actual electrode because of the implanted region under the electrode. Thus, equations 3.2a and 3.3 are modified for two-phase devices,

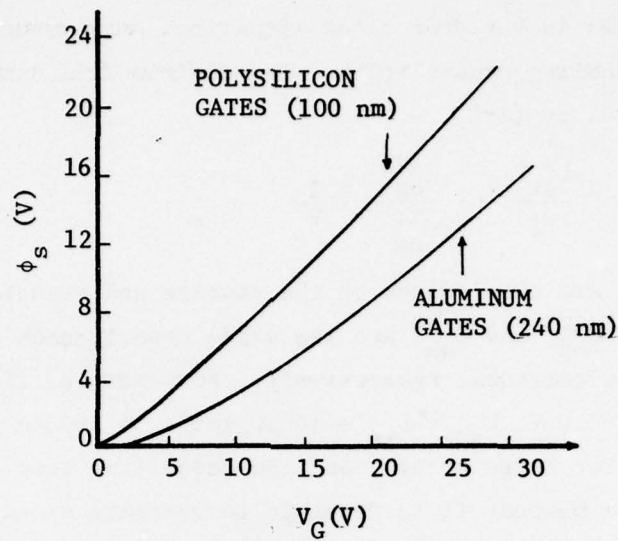
$$Q'_n = \phi_b C_{ox}^{st} A_{st} \quad (3.4)$$

and

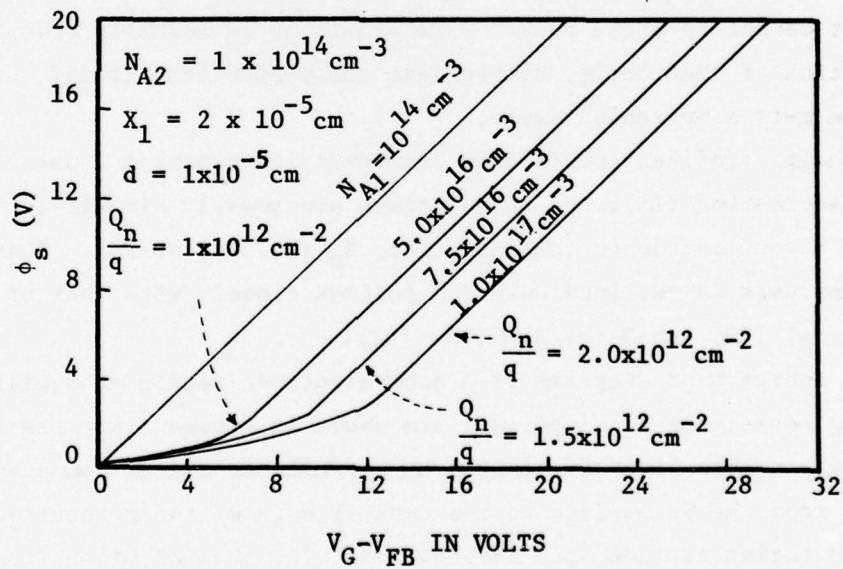
$$I_{s_{2\phi}} = \phi_b C_{ox}^{st} A_{st} f_c \quad (3.5)$$

where ϕ_b is the barrier height, C_{ox}^{st} is the oxide capacitance of the storage electrode, and A_{st} is the area of the storage electrode. Note from Fig. 3.3 that the barrier potential ϕ_b increases with electrode voltage.

In two-phase clocking using symmetrical waveforms shifted by 180° , the fall time is very important. In an idealized square pulse system, there can not be any waveform overlap unless one clock waveform is distorted and lengthened in time. This "drop" clock situation is illustrated in Figure 3.1d. In the normal situation, it is possible that both adjacent electrodes may simultaneously be at the minimum or "rest" potential, V_R . The potential barrier, ϕ_b , is much less for the rest potential case (nominally approximately 5 volts) than it is for an applied electrode bias of $V_R + V_p$ (nominally approximately 15-20 volts). Thus an overlap situation, in which the sending electrode voltage does not decrease significantly until the next potential well begins to form, would increase the signal handling capability. Proposed overlap schemes include stepped clock pulses (88) where the maximum potential is not brought immediately to the rest potential, but is left at an intermediate potential for a period of time. This method, however, decreases the signal handling capability to an extent dependent on the magnitude of the intermediate potential. Non-stepped clock pulses (88) or "push" clock pulses (89) have been proposed where a finite



(a) Stepped oxide method (after 30).



(b) Ion implanted method (after 46).

Figure 3.3. Surface potential curves for 2-phase CCD's with process generated potential barriers.

fall time is used as shown in Fig. 3.1e. The potential barrier ϕ_b can be made larger than in the drop clock situation, with associated greater signal handling capabilities. The minimum fall time for a push clock is given by (89)

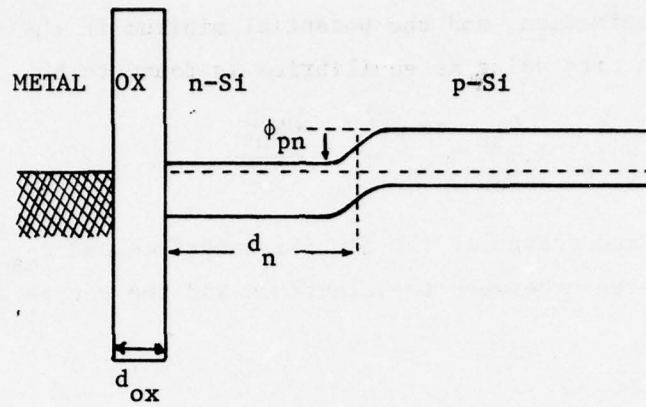
$$t_{f \min} = 2 \frac{L_{st} L_{tr}}{\mu_s} \cdot \frac{C_{ox}^{st}}{C_{ox}^{tr}} \cdot \frac{1}{V_p} \quad (3.6)$$

where L_{st} and L_{tr} are the lengths of the storage and transfer electrode, respectively, and C_{ox}^{st} and C_{ox}^{tr} are the oxide capacitances of the storage and transfer electrodes, respectively. For example, if $d_{ox}^{st} = 100$ nm, $d_{ox}^{tr} = 300$ nm, $V_p = 10$ V, $L_{st} = L_{tr} = 10$ μ m and $\mu_s = 500$ cm²/V sec, then $t_{f \min} = 1.2$ ns. For large arrays, and the associated long clock lines, it is questionable whether it is feasible to generate clock pulses with 1.2 nsec fall times - especially for on-chip clock generators.

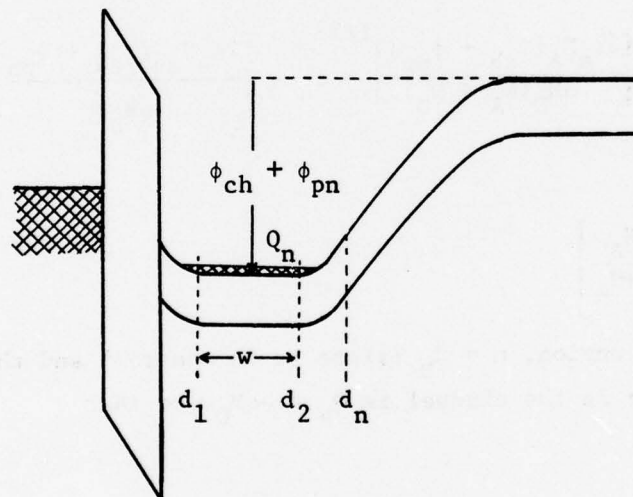
3.1.2. Signal handling capabilities of BCCD's. As indicated in chapter 2, there are currently two basic BCCD structures. One contains a uniformly doped epitaxial n-type layer while the second has a profiled n-type region in which the surface donor concentration is greater than that deeper into the bulk. This profiling is normally done by ion implantation of phosphorus, either into the p-substrate itself, or into a surface n-type epitaxial layer.

Although profiled BCCD's have been analyzed assuming a Gaussian donor distribution (15), the calculations are greatly simplified, assuming a constant donor concentration, N_D (13, 14, 90-94). This latter analysis is outlined here and follows closely with that of Moshen et al (90) and Barbe and Saks (92).

The energy band diagrams of a BCCD electrode region at equilibrium and containing a charge, Q_n , are shown in Figure 3.4. The thickness of the n-type layer is denoted by d_n while d_1 and d_2 represent the distance from the Si surface to the channel edge of the respective depletion region as indicated in Fig. 3.4. The channel width itself



a)



b)

Figure 3.4. Energy band diagram for BCCD a) at equilibrium and b) under bias with charge Q_n in channel.

is denoted by w . The one-dimensional Poisson equation is solved using the depletion approximation, and the potential minimum in the channel, ϕ_{ch} , with respect to its value at equilibrium is found to be

$$\phi_{ch} = V_G - \phi_{ms} + \frac{Q_{ss}}{C_{ox}} - \frac{qN_D d_1^2}{2\epsilon_s} - \frac{qN_D d_1}{C_{ox}} \quad (3.7)$$

where Q_{ss} is the fixed charge at the SiO_2/Si interface and ϕ_{ms} is the work function difference between the electrode and the n-type surface layer.

From Fig. 3.4,

$$d_1 = d_2 - w \quad (3.8)$$

where

$$d_2 = d_n - \left[\frac{2\epsilon_s N_A (\phi_{ch} + \phi_{pn})}{qN_D (N_A + N_D)} \right]^{1/2} = d_n - \left[\frac{2\epsilon_s N_{eq} (\phi_{ch} + \phi_{pn})}{qN_D^2} \right]^{1/2} \quad (3.9)$$

and

$$N_{eq} = \left[\frac{N_D N_A}{N_D + N_A} \right] \quad (3.10)$$

In the channel region, $n = N_D$ (since it is neutral) and thus the charge per unit area in the channel is $Q_n = -qN_D w$ so that

$$w = \frac{-Q_n}{qN_D} \quad (3.11)$$

Equations 3.7 to 3.11 are solved for ϕ_{ch} . The results are expressed in terms of

$$\frac{1}{C_{eff}} = \left(\frac{1}{C_{ox}} + \frac{d_n}{\epsilon_s} - \frac{Q_n}{q\epsilon_s N_D} \right) \quad (3.12a)$$

and

$$V_I = qN_D d_n \left(\frac{d_{ox}}{\epsilon_{ox}} + \frac{d_n}{2\epsilon_s} \right) \quad (3.12b)$$

The parameter V_I is the voltage which must be applied across the p-n junction to deplete the channel. Figure 3.5 shows results of calculations using Eq. 3.11 for the two combinations of N_A , N_D , and n . For the example of 3.5b, and a gate voltage swing from -2 to +5 volts, a full well corresponds to $Q_n/qN_D d_n \sim 0.75$ which gives $Q_n \sim 6.8 \times 10^{11}$ electrons/cm².

The maximum signal charge that can be handled in a bulk channel device is smaller than that of a comparably sized surface channel device mainly because of the decreased effective capacitance of the bulk channel device. The ratio of the maximum charge handling capability of the surface channel versus the bulk channel has been approximated as (14, 90, 93)

$$\frac{Q_{ns}}{Q_{nB}} = 1 + \frac{\epsilon_{ox} d_n}{2\epsilon_s d_{ox}} \quad (3.13)$$

so that the bulk signal charge capacity decreases as the depth of the channel increases. For example, for $d_{ox} = 150$ nm and $d_n = 1$ μ m, the ratio of Q_{ns}/Q_{nB} is 2. Using a Gaussian distribution, similar ratios have been achieved experimentally with deeper junction depths (~ 2.1 μ m). (26). An approximate graphical comparison of charge handling capacity between the various bulk channel devices has been calculated (94) as shown in Figure 3.6. Comparisons of Figs. 3.2 and 3.6 give the differences in charge handling capabilities of surface and bulk channel devices.

Figure 2.9 shows the charge distribution of an implanted bulk channel device. Since $n = N_D$ in the channel region and N_D increases toward the surface, the maximum charge density moves closer to the surface with increasing signal level. It is noted that in contrast

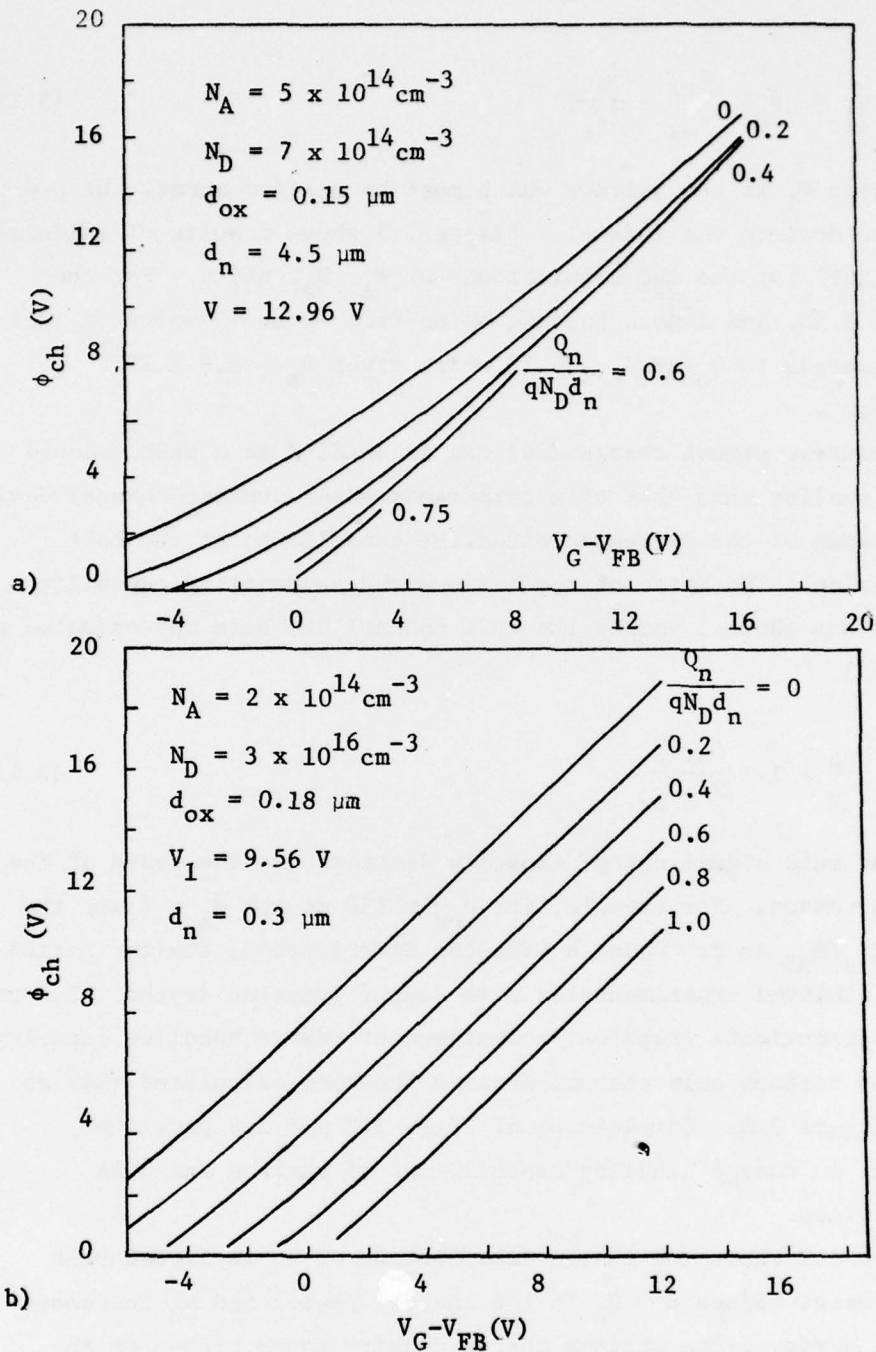


Figure 3.5. Channel potential as a function of gate voltage for two BCCD's assuming constant doping level in the n-type channel region. The results of (a) are applicable to an epitaxial n-region while those in (b) are a reasonable approximation to an ion-implanted region (after 91, 92).

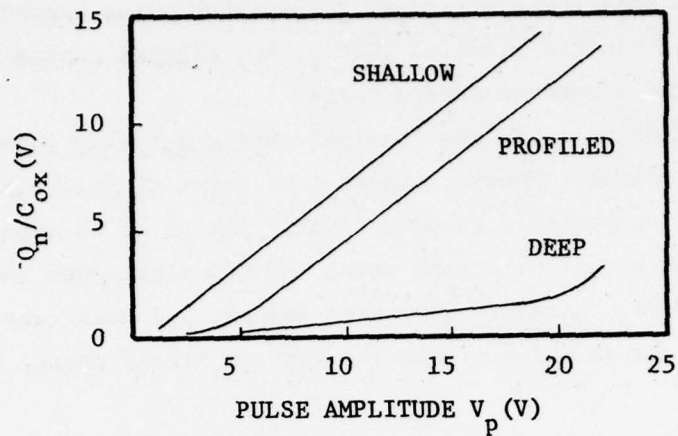


Figure 3.6. Charge handling capabilities of various bulk channel CCD's (after 94).

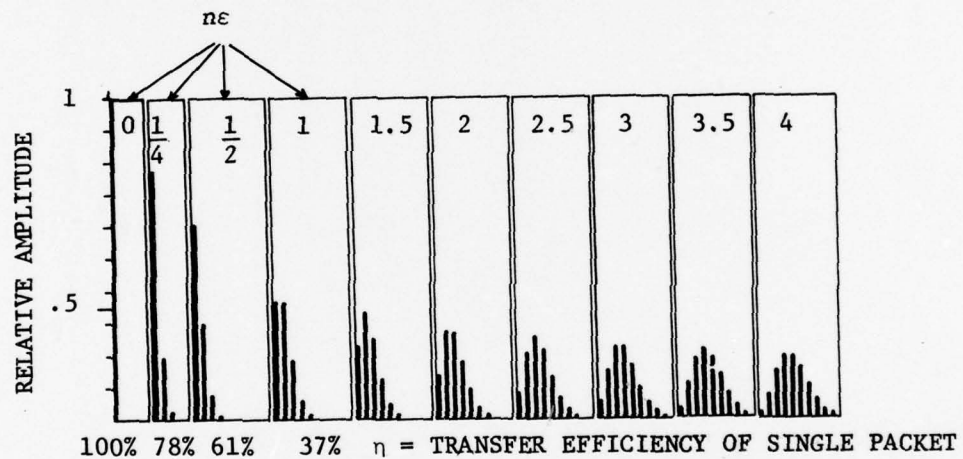


Figure 3.7. Influence of transfer inefficiency product $n\epsilon$ on output signal for a single charge packet input followed by ZEROS. (after 95).

to SCCD's the voltage drop across the oxide decreases as Q_n increases and the maximum charge in the BCCD is limited by avalanche breakdown of the Si between adjacent electrodes, rather than oxide breakdown as for an SCCD. Since in the profiled BCCD's, the highest doping is at the Si surface, the breakdown occurs there.

In this discussion, only the internal charge handling capacity of CCD's was considered. However, because of input circuit limitations, it may not be possible to electrically inject or to optically excite the maximum amount of charge which the CCD electrodes can handle. Furthermore, thermally generated charge, and dark currents will supply some charge and decrease the maximum signal charge handling capability.

3.2. Transfer Inefficiency

An important feature of a CCD is its ability to transfer charge from one electrode to another while maintaining the integrity of the charge packet. However, the charge transfer is not complete and requires a finite time. Since, in each transfer, some charge is left behind, incomplete charge transfer limits the total number of transfers allowable before the signal charge loses its information. The time allotted for charge transfer affects the magnitude of the incomplete transfer so that the frequency response of a CCD depends on the amount of incomplete charge transfer which can be tolerated. The transfer efficiency, η , is defined as the fraction of charge transferred between adjacent storage electrodes. Since η is typically on the order of 0.9999, it is more convenient to discuss the transfer inefficiency, $\epsilon = 1 - \eta$, defined as the fraction of charge lost per transfer between storage electrodes.

3.2.1. General considerations. If the transfer inefficiency is constant, i.e. if it is independent of position and magnitude of the signal charge (this is only approximately true), the effect of transfer inefficiency can be easily calculated. If a single packet of charge is injected into the input of a CCD, the charge will decay exponentially as it propagates. For a CCD of n stages, the output charge will have decayed to $e^{-n\epsilon}$ of its initial value. However, the charge lost from the signal packet due to incomplete transfer is kept in the sending stage and a fraction η of this is transferred during the next clock pulse with ϵ of this charge remaining. As the signal charge packet moves down the CCD then, a dribble of charge follows in subsequent time periods. Figure 3.7 represents calculated outputs of a CCD with n stages and constant ϵ , with $n\epsilon$ as a parameter (95). In each case the charge corresponding to the CCD output in the output time period for the injected signal (the injection time delayed by n clock pulses) is indicated on the left. Charge output at subsequent time

periods are indicated progressively to the right. It is noted that for $n\epsilon > 1$ most of the charge is detected in packets other than the signal packet. At larger values of $n\epsilon$, the envelope of the output pulse train approaches a Gaussian distribution. Consider a digital shift register in which the output detector is set at 61% of the injected charge for a ONE indication. The $n\epsilon$ product must then be less than 0.5. For a relatively short shift register of 100 cells (which requires 300 transfers for a 3-phase system) to transfer adequate input signal to the output node, ϵ must be less than 0.0017. To achieve longer digital shift registers, signal regeneration circuits can be used periodically in the register.

In addition to the incomplete transfer described, the signal can be degraded by interaction of charge with interface or bulk traps. If these traps are empty any charge in the channel will fall into them almost instantaneously thus filling them, but it requires a relatively long time for the electrons to be thermally excited from the traps back into the channel. Let δ represent the fixed charge loss per transfer, i.e. that fraction of the charge of an injected logical ONE which is lost to these traps on each transfer. Then in a register of n stages, $n\delta$ is lost in the transfer. If $n\delta > 1$ all of the charge is lost and charge from subsequent ONE's will be lost to fill the remaining traps. The value of δ depends on the number of empty traps and thus depends on the time since a ONE was transferred.

The combination of transfer inefficiency and fixed charge loss can be used to describe the CCD operation. Although the trapped charges are re-emitted, the process is so slow that this contribution to transferred charge is neglected. The randomness of this emission, however, does contribute to noise. Figure 3.8 illustrates the degradation involved in the passage of a string of ten consecutive ONE's after a series of ZERO's. Various values of ϵ , δ , and n are used as parameters. If, instead of using an empty packet to represent a ZERO, a fixed background charge is used, the traps are continuously being filled, and δ is reduced substantially. This background bias charge is referred to

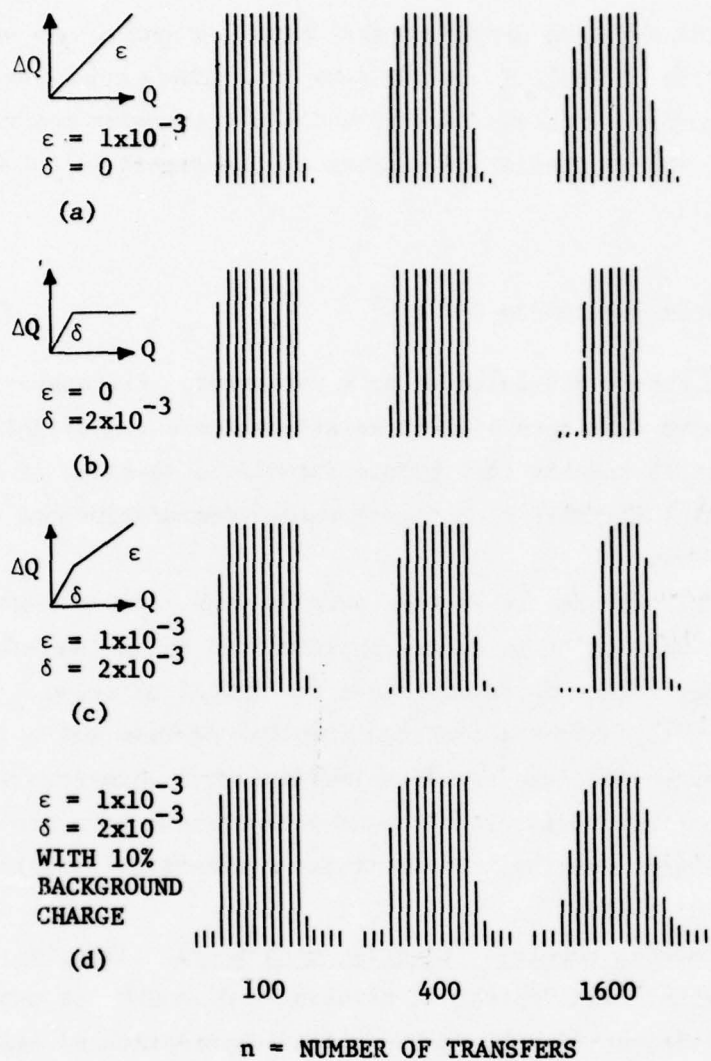


Figure 3.8. Calculated results of ten ONE's after a series of zeros as a function of various ϵ , δ , and n values for 100, 400, and 1600 transfers respectively (after 9).

as a FAT ZERO in SCCD's. In BCCD's the effects of interface traps are eliminated and a smaller bias charge (SKINNY ZERO) is often used to represent a zero.

This discussion has been geared toward digital signals, yet one important application of CCD's is in the area of analog signal processing. Using z-transforms a closed-form solution for transfer inefficiency was derived (96). The amplitude attenuation of the signal as a function of frequency is (97)

$$\frac{S_{out}}{S_{in}} = \exp[-n\epsilon(1 - \cos 2\pi f/f_c)] \quad (3.14)$$

This is plotted in Figure 3.9 using $n\epsilon$ as a parameter. Although other authors (98, 99) have developed similar relationships using slightly different mathematical models, this simple formula is adequate in most cases to give a quick estimate of the performance degradation due to transfer inefficiency.

In practical situations, it is desirable to keep ϵ and δ minimized to decrease signal distortion in analog applications and to maximize the number of elements between regenerators in digital circuits. It is, thus, necessary to analyze the charge transfer process and to determine the mechanisms which cause transfer inefficiency. Numerous analyses using different assumptions and boundary conditions have been published. In the next section, some of these mathematical models and their results are discussed.

3.2.2. Mathematical models of transfer mechanisms. Although the physical structure and basic operating principles of a CCD are conceptually quite simple, an accurate mathematical description of transfer characteristics is difficult to derive. Approximations are normally used to simplify both the detailed model and the solution of the differential equations describing the model.

The basic equations to be solved, along with the boundary conditions are the continuity equations for holes and for electrons,

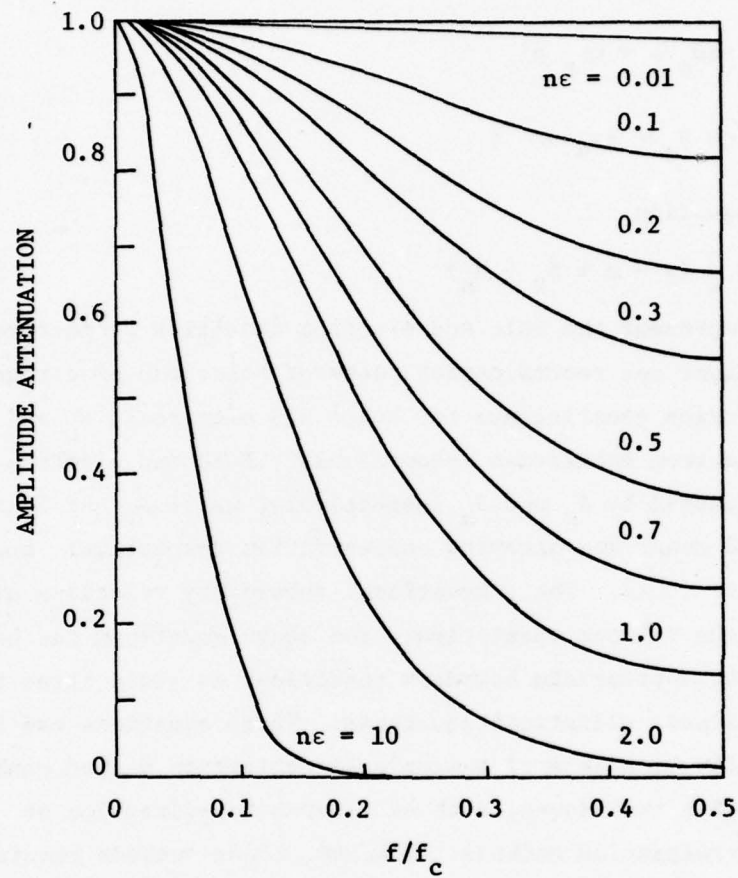


Figure 3.9. Amplitude attenuation of a CCD transfer function as a function of frequency with transfer inefficiency product $n\epsilon$ as a parameter (after 95).

$$q \frac{\partial p}{\partial t} = -\nabla \cdot J_p - qR_p \quad (3.15)$$

$$q \frac{\partial n}{\partial t} = \nabla \cdot J_n - qR_n ; \quad (3.16)$$

the transport equations for holes and electrons,

$$J_p = -qD_p \nabla p + q\mu_p p\xi \quad (3.17)$$

$$J_n = qD_n \nabla n + q\mu_n n\xi ; \quad (3.18)$$

and Poisson's equation

$$\nabla \cdot \xi = \frac{q}{\epsilon} (p - n + N_D - N_A) \quad (3.19)$$

where p and n represent the hole and electron densities respectively. R_p and R_n represent net recombination rates of holes and electrons, D_p and D_n are diffusion coefficients for holes and electrons, μ_p and μ_n are hole and electron mobilities respectively. Hole and electron current densities are denoted by J_p and J_n respectively, while N_D and N_A represent the ionized donor and acceptor concentration respectively and ξ is the electrostatic field. The conventional subsidiary relations are used to relate the various quantities. The above equations can be combined with the appropriate boundary conditions to yield three two-dimensional nonlinear elliptical equations. These equations can be solved numerically by a form of Newton's linearization method combined with some iterative techniques, such as alternating-direction or successive over-relaxation methods. However, these methods require large computer storage and extensive computation time, and thus many simplifying assumptions have been made.

The approximations which have been used are listed below.

1. One-dimensional, or combinations of one and two-dimensional analyses: most early analyses are one-dimensional, either along the surface or perpendicular to the surface. To obtain more accurate electric field results, some contributors have solved Poisson's

equation in two-dimensions while using a one-dimensional form of the continuity and transport equations. Others use Eq. 2.8 to determine the relationships between surface potential and signal charge.

2. Static conditions, or approximate time independence.
3. Small (or zero) concentration of mobile minority carriers: This greatly simplifies the analysis but neglects the influence of the signal charge on the potential magnitude and distribution.
4. Instantaneous redistribution of majority carriers: Most analyses neglect the majority carrier equations and assume that the majority carriers can redistribute themselves instantaneously after changes in minority carrier densities and depletion layer widths.
5. Depletion approximation: Many analyses assume that the depleted regions are completely devoid of mobile carriers and that abrupt transitions occur in mobile carrier densities at the edges of the depletion region.
6. Majority carrier distribution is determined by one-dimensional depletion approximation.
7. Minority carriers located exactly at potential energy minimum: Usually the minority carrier concentration is assumed to be a delta function at, or a rectangular distribution centered around, the potential energy.
8. No surface effects, charge trapping, etc.
9. Gradual channel approximation: This assumes that the electric field perpendicular to the surface is much larger than the electric field parallel to the surface. This assumption is not valid at the edges of the electrodes since it eliminates fringing field contributions.
10. Fringing electric fields caused by the adjacent electrodes are either considered to be zero, a constant, or a given reference (100).
11. Infinite minority carrier sink at interface between sending and receiving electrodes: This boundary condition greatly simplifies the analysis and is relatively valid for small and medium size

charge packets but does not account for "charge bunching" in the receiving electrode.

12. Uniform surface state density and capture cross-section: If surface state density and capture cross-section is considered, their energy dependence is neglected.
13. Fringing fields included as linear combination in transport equation: In the basic set of semiconductor equations, it is assumed that the drift and diffusion contributions can be expressed as additive terms in the transport equation which thus linearizes these effects. Some of the significant analyses are summarized in Table 3.1. As is evident, numerous methods have been attempted, but a complete analysis has yet to be accomplished. The results of these and other analyses are discussed later.

Other techniques have been used to model the various effects leading to transfer inefficiency in CCD's. A lumped charge model has been developed (101, 102) which characterizes the dynamics of charge transfer in terms of single-device, small-signal characteristics. Three contributions to incomplete transfer which are common to all types of CCD's are a) an intrinsic transfer rate contribution based on the mechanisms of free charge transfer, b) an output conductance or feedback contribution, c) a modulation of the storage capacitance of the sending electrode. Other effects such as effects of interface states can be incorporated into this model. Figure 3.10 shows a schematic representation of the lumped charge model. In (a) a charge packet is shown in a well under a single electrode which we will refer to as the sending or source electrode. At a certain time, the receiving, or drain electrode is turned on and the charge is transferred from source to drain. Let $\phi_{ss}(t)$ and $\phi_{sd}(t)$ be the electrostatic surface potential at the Si surface in source and drain regions respectively. Let ϕ_{sso} and ϕ_{sdo} represent the respective source and drain surface potentials for empty wells (but with the clock voltages applied for transfer). Then

Ref. #	Year	Surface or Bulk	Phases	Dimensions	Static or Dynamic	Gradual Channel Approx.	Infinite Sink Boundary	Drift (Dr), Diffusion (Di) or Fringing Field (ξ_y) considerations	ξ_f Considerations	Potential Considerations	APPROACH	NOTES
8	1970	S	2	1	D	Yes		Dr		Eq.2.8	Continuity	
133	1971	S		1	D	Yes	Yes	Dr,Di		Eq.2.8	Continuity Transport	A
104 134	1971	S	3	1	D	Yes	Yes	Dr,Di		Eq.2.8	Transport	B
100	1971	S	3	1	S	Yes		All	Formula			C,D,E
20	1972	S	3	1,2	S		Yes	Dr,Di	Poisson		2-D Poisson 1-D Continuity	F
135	1972	S,B		2	S			Dr,Di			2-D Poisson	C
103	1972	S	3	1	D			All	Numerial		Continuity, Transport	
136	1972	S	2	1	D		Yes	All	Constant		Continuity, Transport	
55	1972	S	2	1	D	Yes	Yes	Dr			Continuity, Poisson	
22 109	1973	S,B	2-3	2	S				Poisson		2-D Poisson	C,D
108	1973	S	2	1,2	D		Yes		Poisson		1-D Continuity Transport 2-D Poisson	
137	1973	B		1	S						Poisson	A
110	1974	S		1,2	D		Yes	All	Constant Varying		1-D Continuity 2-D Poisson	G
106	1974	S		1,2				All	Poisson	Poisson	1-D Continuity 2-D Poisson	

105 107	1974	S	2	1,2		Yes	All	Poisson	Linear Approx	1-D Continuity Transport 2-D Poisson	A
21	1974	S		2	D		All	Formula	Poisson	Transport Continuity Poisson	A,H
138	1974	S		2	D					Poisson, Particle Model	H,I
139	1974	S	3	1	D		All	Carne's Eqn.	Eq.2.8.	Continuity Transport	
112	1974	B	4	2	S					Poisson	J
140	1974	B		1	S	Yes				Poisson	K
93 141	1974	B		1	S					Poisson	K,L
142	1975	S,B		1	D		All			Continuity Transport	
16	1975	B	2,3	2	S					Poisson	M
143 141	1975	S	3	1	D	Yes	D_i, ξ_f	Carne's Eqn.	Fourier Series	Continuity	N
145	1975	S	3	1	D		All	Carne's Eqn.	Eqn.	Transport Continuity	O
163	1976	S	4	2	S		ξ_f	Green's Function		Green's Function	P
144	1976	B		1	S			Poisson			

Notes: A) Finite difference method, B) Use of effective diffusion constant, C) Assumes zero mobile minority charge, D) Fourier series solution, E) Use of formula for fringing fields, F) Use of effective carrier velocity, G) Consideration of constant and spatially varying fringing field, H) Consideration of signal charge, I) Use of Fourier transform, J) Fourier series for case of finite charge, K) Uniform doping of layer, L) Gaussian doping of layer, M) Obtains average potential solution using one-dimensional equation, N) Use of variation method, O) Fringing field considered only during and after turn off, P) Assumes no oxide charge, and all gates lie on same plane.

Table 3.1. Summary of CCD Analyses

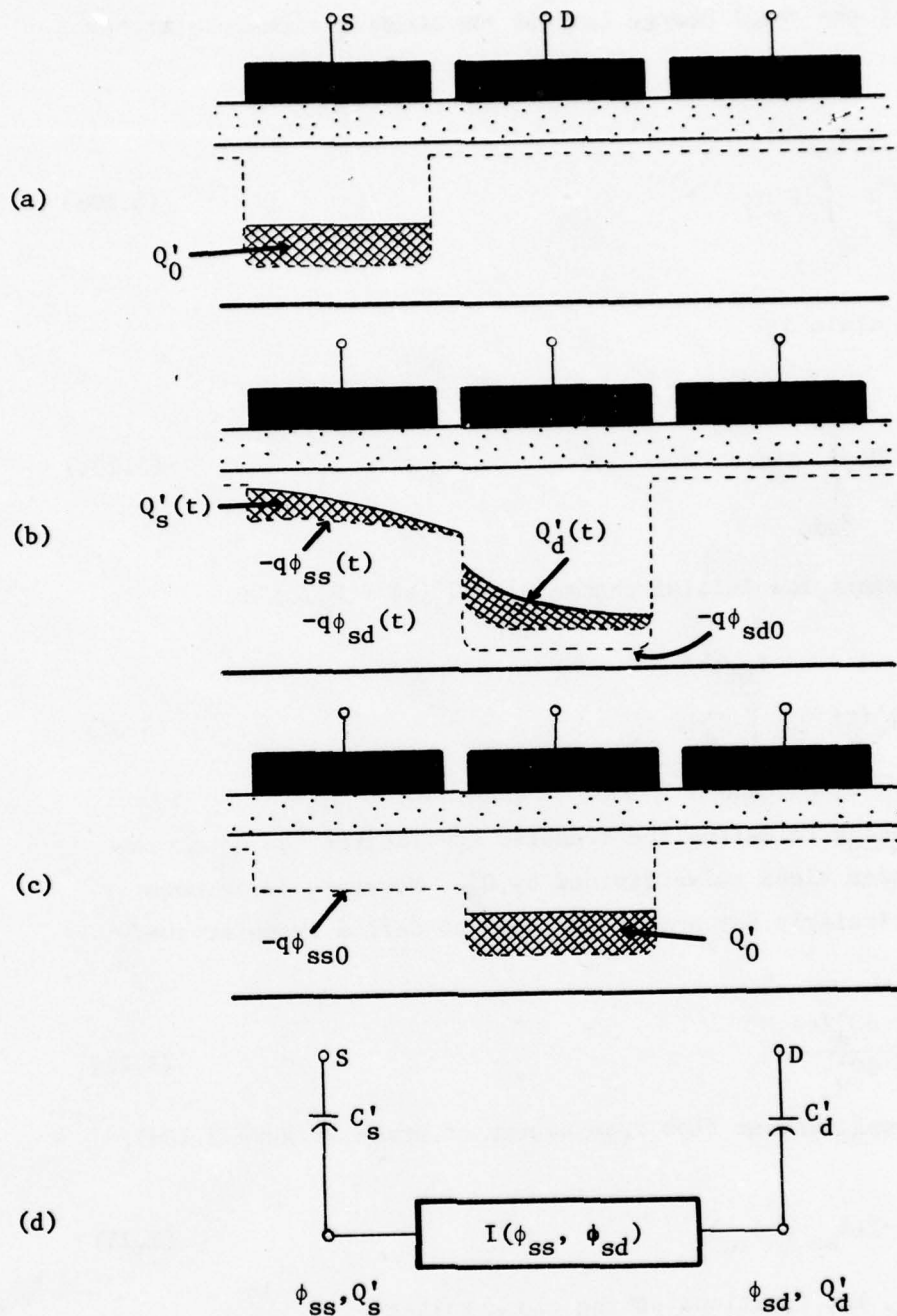


Figure 3.10. Illustration of charge transfer, and equivalent circuit for lumped charge model.

since $C' = \left| \frac{dQ'}{d\phi} \right|$ the total charge left in the sending electrode at any time t is

$$Q'_s(t) = \int_{\phi_{sso}}^{\phi_{ss}(t)} C'_s d\phi \quad (3.20a)$$

and that in the drain is

$$Q'_d(t) = \int_{\phi_{sdo}}^{\phi_{sd}(t)} C'_d d\phi \quad (3.20b)$$

Letting Q'_o represent the initial charge $Q'_o = Q'_s(t) + Q'_d(t)$ or

$$Q'_o = Q'_s(t) + \int_{\phi_{sdo}}^{\phi_{sd}(t)} C'_d d\phi \quad (3.21)$$

It would be tempting to define the transfer inefficiency as Q'_s at the end of the transfer clock pulse divided by Q'_o . However, it is more convenient, particularly for analog systems, to define transfer inefficiency as

$$\epsilon(t) \equiv \frac{dQ'_s(t)}{dQ'_o} \quad (3.22)$$

Letting I represent current flow from source to drain (Figure 3.10d),

$$\frac{dQ'_s}{dt} = -I(\phi_{ss}, \phi_{sd}) \quad (3.23)$$

where ϕ_{ss} and ϕ_{sd} are functions of the clock voltages.

Differentiating Eq. 3.22 with respect to time gives

$$\frac{d\varepsilon(t)}{dt} = \frac{d(dQ'_s/dt)}{dQ'_o}$$

since Q'_o is fixed in a given transfer. Combining this with Eq. 3.23 gives

$$\frac{d\varepsilon(t)}{dt} = \frac{\partial I}{\partial \phi_{ss}} \frac{d\phi_{ss}}{dQ'_o} - \frac{\partial I}{\partial \phi_{sd}} \frac{d\phi_{sd}}{dQ'_o} \quad (3.24a)$$

Defining instantaneous transconductance, g_m as $\frac{\partial I}{\partial \phi_{ss}}$ and instantaneous reverse transfer conductance, g_r as $\frac{\partial I}{\partial \phi_{sd}}$ gives

$$\frac{d\varepsilon(t)}{dt} = g_m \frac{d\phi_{ss}}{dQ'_o} - g_r \frac{d\phi_{sd}}{dQ'_o} \quad (3.24b)$$

Combining Eqs. 3.20a and 3.22 gives

$$\frac{d\phi_{ss}}{dQ'_o} = \frac{\varepsilon(t)}{C'_s} - \frac{1}{C'_s} \int_{\phi_{sso}}^{\phi_{ss}} \frac{dC'_s}{dQ'_o} d\phi \quad (3.25)$$

From physical arguments we can approximate

$$C_D \approx \frac{dQ'_o}{d\phi_{sd}} \quad (3.26)$$

and from Eqs. 3.24b, 3.25 and 3.26 we can write

$$\varepsilon(t) = \frac{C'_s}{g_m} \frac{d\varepsilon(t)}{dt} + \frac{g_r}{g_m} \frac{C'_s}{C'_D} + \int_{\phi_{sso}}^{\phi_{sd}(t)} \frac{dC'_s}{dQ'_o} d\phi \quad (3.27)$$

Equation 3.27 is a linear differential equation with a solution of the form

$$\varepsilon(t) = \varepsilon_i + \varepsilon_D + \varepsilon_C \quad (3.28)$$

where

$$\epsilon_i(t) = \exp\left[-\int_0^t \frac{g_m}{C'_s} dt\right] \quad (3.29)$$

is the intrinsic transfer limitation of the device,

$$\epsilon_D(t) = \left[\frac{g_r C'_s}{g_m C'_D}\right] \quad (3.30)$$

is the feedback contribution, and

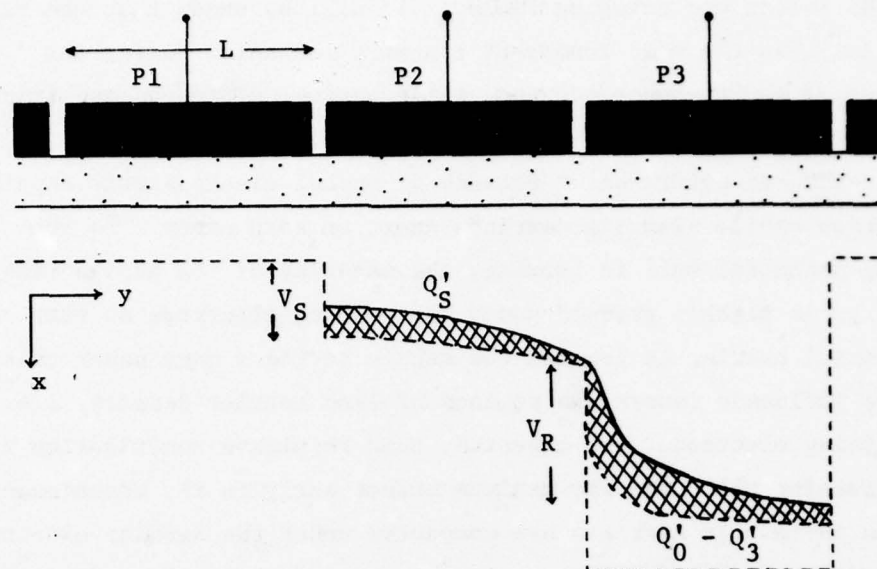
$$\epsilon_C(t) = Q'_s(t_0) \frac{1}{C'_s} \frac{dC'_s}{dQ'_0} \quad (3.31)$$

is the variation of the source storage capacitance with source potential.

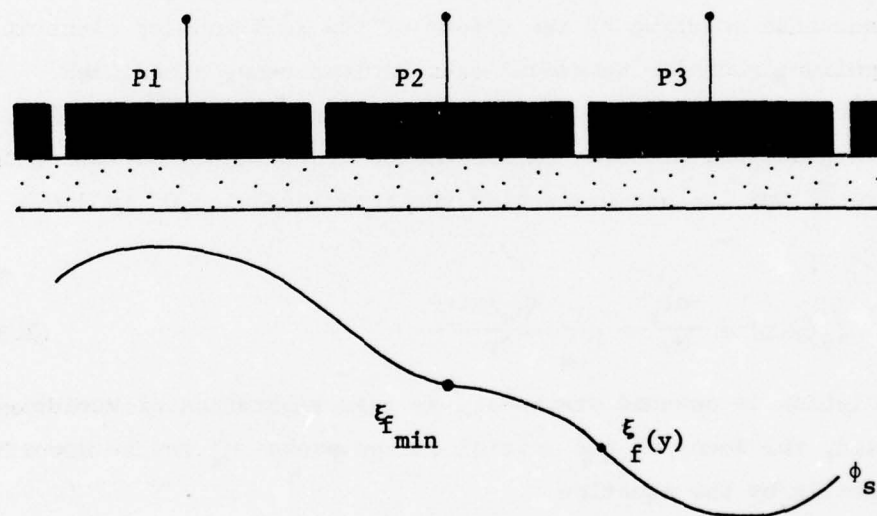
3.2.3. Kinetics of free charge transfer. An important characteristic of a CCD is its ability to transfer mobile charge from one potential well to another. The allowable clock frequencies and the number of stages in a register are influenced by the efficiency and speed of this free charge transfer.

A variety of physical structures fabricated by several processing methods have been investigated, both experimentally and theoretically, for various operating conditions. Here the discussion of the transfer characteristics of CCD's is limited to two-phase and three-phase SCCD's and BCCD's operating in the complete and in the incomplete transfer modes. The effects of self-induced drift, thermal diffusion, fringing fields, background or bias charge, clock waveforms and device processing are discussed.

3.2.3.1. Kinetics of complete charge transfer. Most CCD's operate in the complete charge transfer mode in which there are no potential barriers in the path of the charge packet behind which some of the minority charge can be trapped. Thus, depending on device conditions, practically all of the minority charge will transfer from one potential well to another. Figure 3.11 is a hybrid schematic used to analyze the complete charge transfer mode. There are three basic mechanisms which assist in the charge transfer: self-induced drift,



(a) Free charge hybrid schematic using abrupt potential transitions.



(b) Potential profile for modelling fringing fields.

Figure 3.11. Models for complete charge transfer mode.

thermal diffusion and fringing fields. It will be shown that the self-induced drift is the most important transfer mechanism during the early part of the transfer process, while thermal diffusion and fringing fields contribute during the latter stages.

Self-induced drifts occur because of mutual electrostatic repulsive forces which mobile minority carriers exert on each other. As the receiving potential well is forming, the majority of the mobile minority charge is tightly grouped under the sending electrode so that as the potential barrier is lowered the mobile carriers move under this repulsive influence toward the regions of less carrier density, i.e. the receiving electrode. As expected, this repulsive contribution to charge transfer will have its maximum effect early in the transition time when the mobile carriers are compacted under the sending electrode and will decrease in significance as the carriers leave the electrode region. For sufficiently large charge packets, the transfer is initially dominated by this self-induced drift effect.

An accurate solution of the effect of the self-induced electric field requires extensive numerical calculations using a modified Boltzmann transport equation. However, the magnitude of the self-induced longitudinal electric fields can be approximated by taking the derivative of Eq. 2.8 and neglecting the term involving Q_n in the brackets:

$$\xi_y(y, t) = \frac{-d\phi_s}{dy} = \frac{1}{C_{ox}} \frac{\partial Q_n(y, t)}{\partial y} \quad (3.32)$$

If the solution is assumed stationary so that separation of variables may be used, the decay of the initial charge packet Q'_0 may be described asymptotically by the equation

$$\frac{Q'(t)}{Q'_0} = \frac{t_0}{t+t_0} = \frac{1}{1+t/t_0} \quad (3.33)$$

where

$$t_o \sim \frac{\pi L^2 C'_{ox}}{2\mu_n Q'_o} = \frac{\pi L^2}{2\mu_n \Delta\phi_s} \quad (3.34)$$

where $\Delta\phi_s$ is the difference in the surface potential for the charged and uncharged state, or the magnitude of the signal voltage. Using a more accurate integral formulation (103), the maximum self-induced electric field magnitude for uniform charge profiles can be given approximately as

$$E_{y_{max}} \sim 4.5 \times 10^{11} Q_o \text{ V/cm} \quad (3.35)$$

Equation 3.35 provides a simple, though approximate, relationship between the maximum self-induced field and the signal charge concentration. From Eqs. 3.33 and 3.34 it is apparent that the charge decay is faster for larger Q'_o . For small signal charge packets, or after most of the charge has been transferred, Q_n is small in the sending well, and so the self-induced field can be neglected. In this case, electrons are transferred primarily by thermal diffusion. Using the continuity-transport equation with only the thermal diffusion term, and assuming no backward flow of charge, an infinite sink at $y=L$, and uniform initial charge per unit area, Q_o , the charge packet approaches a cosine distribution asymptotically in time (103, 104)

$$Q_n(y,t) = \frac{4Q_o}{\pi} \cos \frac{\pi y}{2L} \exp \left(-\frac{t}{\tau_{th}} \right) \quad (3.36)$$

where τ_{th} is the thermal time constant

$$\tau_{th} = \frac{4L^2}{\pi^2 D_n} \sim \frac{L^2}{2.5D_n} \quad (3.37)$$

where D_n is the diffusivity of electrons in the well and is related to the mobility by the Einstein relation

$$\frac{D_n}{\mu_n} = \frac{kT}{q} \quad (3.38)$$

assuming $L = 10 \mu\text{m}$ and $D_n = 15 \text{ cm}^2/\text{sec}$ (corresponding to $\mu = 580 \text{ cm}^2/\text{Vsec}$), Eq. 3.37 gives $\tau_{th} = 2.7 \text{ nsec}$. For transfer inefficiency of 10^{-4} , 9.2 thermal time constants would be required, or 25 nsec per transfer.

For large charge packets, the initial transfer is primarily by the induced drift field while the final transfer is limited by internal diffusion. The charge at which the induced field becomes negligible is approximately that which is equivalent to an induced voltage of kT/q or

$$Q_{nth} = -C_{ox} \frac{kT}{q} \quad (3.39)$$

For an oxide thickness of 100 nm this corresponds to an electron density of about 6×10^9 per cm^2 . Since this value is one to two orders of magnitude smaller than the signal charge used for many applications, most of the charge is transferred by the induced field. From Eq. 3.34 and an initial electron density of 10^{12}cm^{-2} , t_0 is 0.59 nsec or the initial charge packet is one-half transferred in 0.59 nsec. This compares with the thermal time constant of 2.7 nsec. Because of fringing fields, the potential variation is not a step function at the edge of the wells as shown in Fig. 3.11(a), but is a smooth curve, as illustrated in Fig. 3.11(b). Fringing electric fields increase the transfer speed of the last residues of charge and thus, increase the maximum operating frequency of the CCD. Bulk channel CCD's have significantly larger fringing fields, than surface channel CCD's, and thus have considerable higher frequency response.

The effects of fringing fields can be determined by solving Poisson's equation (numerically) in two dimensions (20, 22, 105-109). An approximate solution has been derived in closed form (100) for the minimum fringing field, which occurs at the center of the transfer electrode if it is held at a potential equal to the average of the adjacent electrodes

$$\xi_{f_{min}} \approx 6.5 \frac{d_{ox} \Delta V}{L^2} \left[\frac{5X_d/L}{5X_d/L+1} \right]^4 \quad (3.40)$$

where X_d is the thickness of the depletion region under the transfer electrode and ΔV is the voltage difference between adjacent electrodes. Another similar equation for calculating the minimum fringing field is (91)

$$\xi_{f_{min}} \approx \frac{2}{3} \frac{\Delta V}{L^2} \frac{\pi \epsilon_s}{C_{eff}} \quad (3.41)$$

where for surface channel CCD's

$$C_{\text{eff}} = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{d_{\text{ox}}} \quad (3.42)$$

and for BCCD's

$$C_{\text{eff}} \approx \left[\frac{d_{\text{ox}}}{\epsilon_{\text{ox}}} + \frac{d_n}{\epsilon_s} + \frac{Q_n/N_D}{2q\epsilon_s} \right]^{-1} \quad (3.43)$$

From these equations, it is seen that the fringing field, and thus speed of charge transfer, increases as the length of the electrode decreases. Charge handling capability is, of course, decreased.

An important parameter in the transfer of the last residue of charge is the single carrier transfer time, t_{tr} (42)

$$t_{\text{tr}} = \frac{1}{\mu_n} \int_0^L \frac{dy}{\xi_f(y)} \quad (3.44)$$

Since $1/\xi_f(y)$ increases almost linearly from the edges to the center of the transfer electrode (100) the average fringing field is about twice the minimum value. The single carrier transit time can then be approximated by

$$t_{\text{tr}} \approx \frac{L}{2\mu_n \xi_{f\text{min}}} \quad (3.45)$$

However, the charge in the receiving well decreases the surface potential there, and thus decreases the fringing field relative to that calculated. As a result, not all of the charge is transferred in a single carrier transit time. After approximately one transfer time, the charge profile becomes stationary and decays exponentially with a final time constant τ_f of the order of $t_{\text{tr}}/3$ (103, 110). An approximate formula for τ_f which includes the effect of thermal diffusion is (110)

$$1/\tau_f \approx K_1^2 \frac{\pi^2 D_n}{4L^2} + \frac{(\mu_n \xi_{f\text{min}})^2}{4D_n} \quad (3.46)$$

where the coefficient K_1 , which varies from 1 to 2, is a function of the fringing field. For zero fringing field, $K_1 = 1$ and $\tau_f = 4L^2/\pi^2 D$ in agreement with Eq. 3.37. The two terms in Eq. 3.46 are comparable for $\xi_{f_{\min}} \approx \frac{\pi kI}{L q}$. For $L = 10 \mu\text{m}$, the charge decay is dominated by the fringing effects for $\xi_{f_{\min}} > 100 \text{ V/cm}$. Since $\xi_{f_{\min}}$ is typically on the order of $10^2 - 10^3 \text{ V/cm}$, (dependent on electrode^{min} length), the final time constant, and thus the operating speed, is largely determined by the fringing fields. The increased speed of BCCD's with respect to SCCD's is a result of the increased fringing fields in the BCCD's.

Figure 3.12 illustrates the results of numerical analysis (105, 107) of a two phase overlapping gate p-channel surface channel structure using a one-dimensional continuity-transport equation and two-dimensional Poisson's equation. The surface potential variation with distance is shown in (a) and the resultant fringing field in (b). Fringing fields of about 10^5 V/cm occur at the edges of the sending and transfer electrodes. In Figure 3.13(a), various combinations of the current densities resulting from self-induced drift, thermal diffusion, and fringing fields are shown which emphasize the importance of the fringing field contribution. The effect of initial charge packet concentration on transfer time is shown in Figure 3.13(b) illustrating that large initial charge packets transfer faster than smaller packets. The influence of the magnitude of the fringing field on transfer inefficiency and transfer speed has been analyzed and is shown in Fig. 3.14 (111). The figure indicates good agreement between the two-dimensional numerical solution of Poisson's equation, with the one-dimensional charge control model solution.

The actual magnitude of transfer inefficiency is a strong function of the design and processing of the particular CCD. Typical data of various types of CCD's is presented here as an example of current capabilities. Figure 3.15 shows transfer inefficiency versus clock

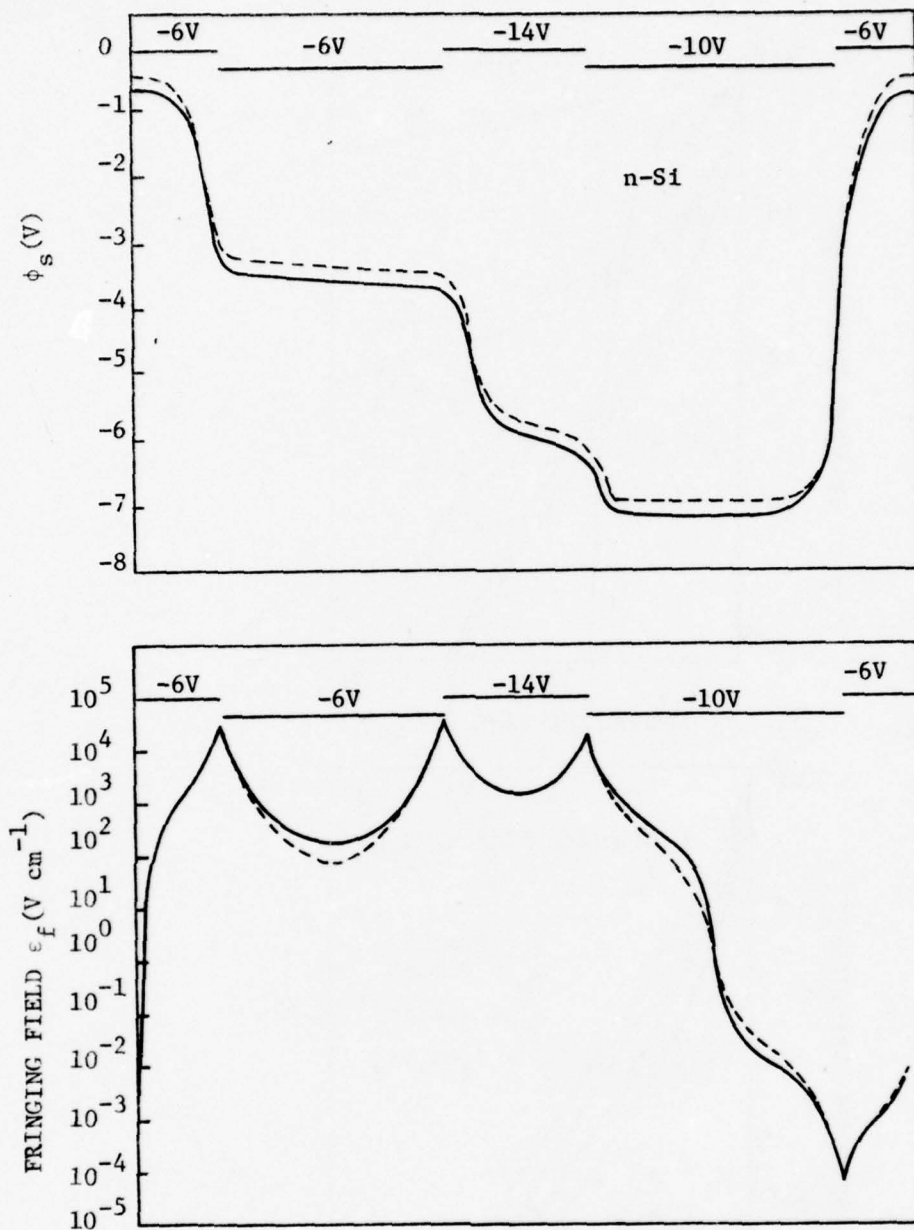


Figure 3.12. Surface potential and fringing field along the surface of two-phase overlapping gate p-channel CCD for substrate doping levels of 5×10^{14} (solid line) and 1×10^{15} (dashed line). For this calculation $d_{st}^{ox} = 100\text{nm}$ and $d_{tr}^{ox} = 300\text{nm}$ (after 105, 107). The results are applicable to n-channel sCCD's with a change in gate polarity.

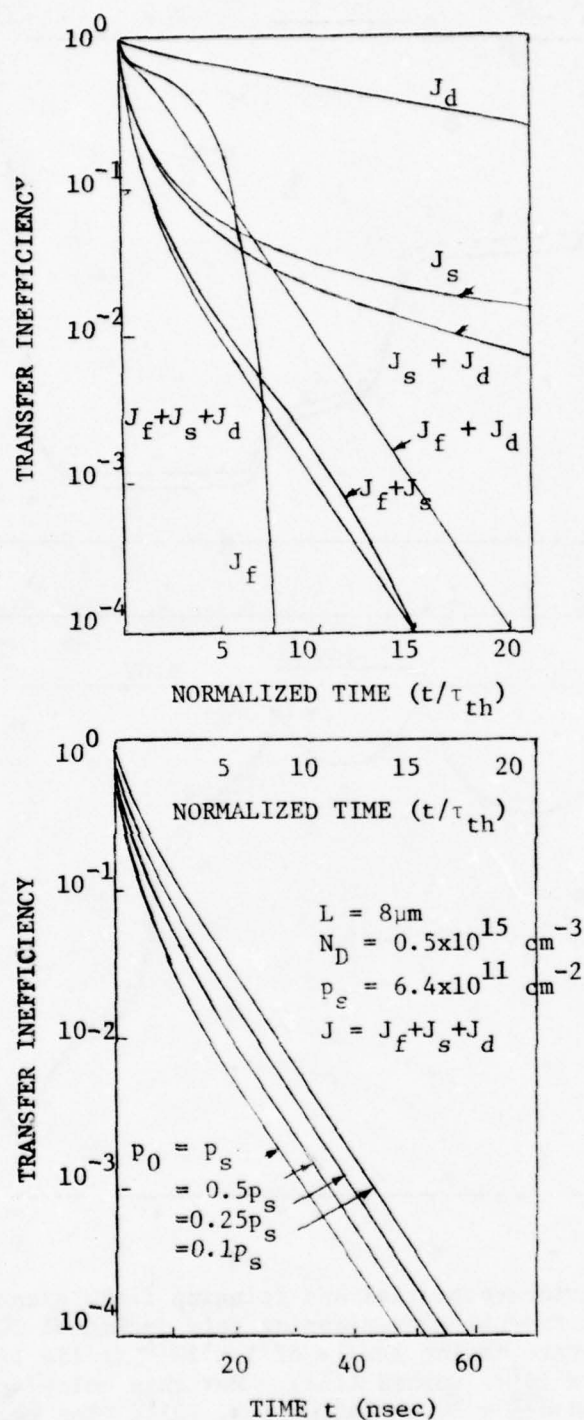


Figure 3.13. Transfer rate characteristics for p-channel SCCD indicating relative importance of self-induced drift, diffusion, and fringing fields (a), and influence of size of initial charge packet (b) (after 105, 107).

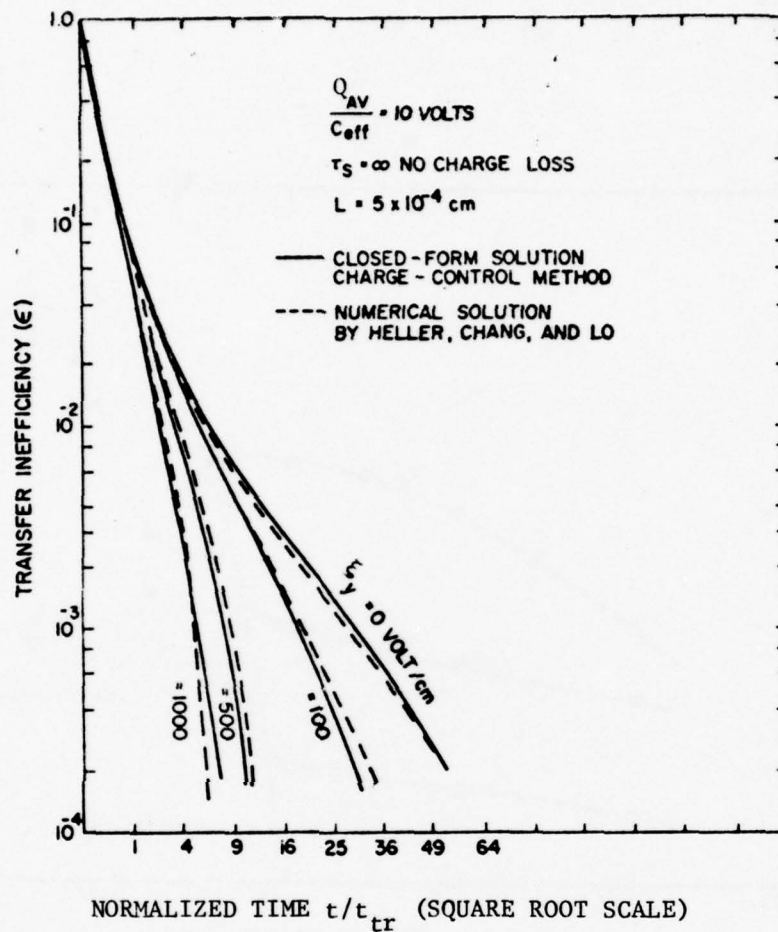


Figure 3.14. Effect of fringing field on the fraction of the charge remaining in the discharging well as a function of time (after 111).

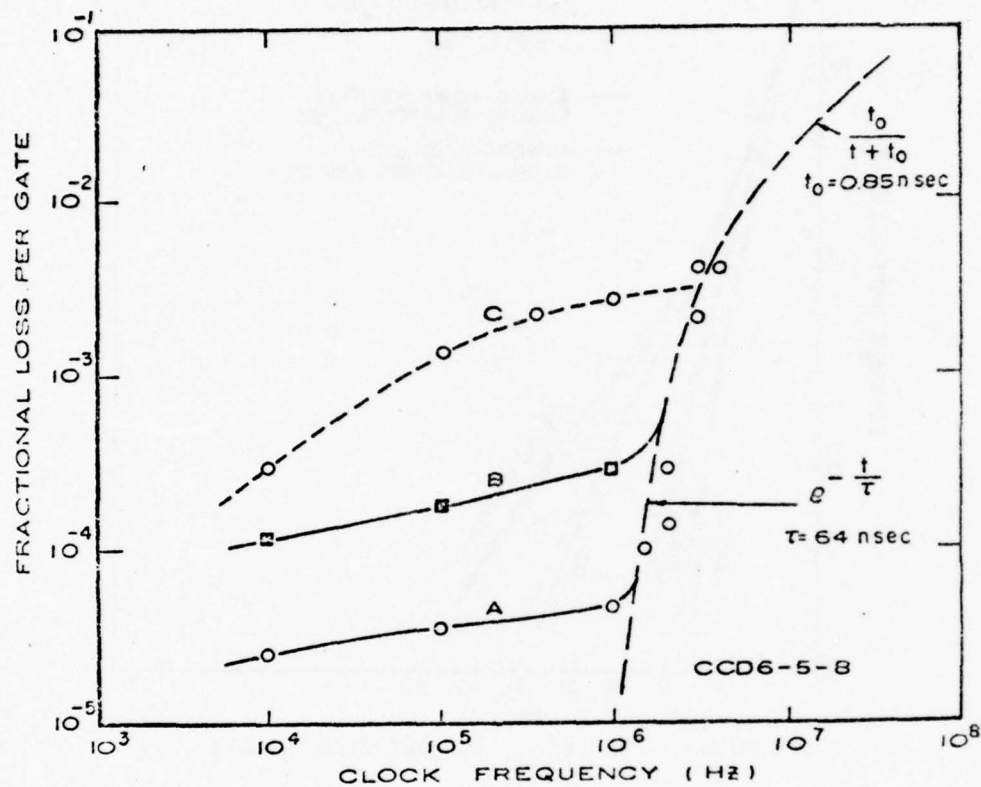


Figure 3.15. Transfer inefficiency (fractional loss per gate) as a function of clock frequency for two-phase overlapping transfer gate CCD's.
 Curve A: 64-stage, 5.0 mil wide gates with 50% FAT ZERO
 Curve B: 128-stage, 0.5 mil wide gates with 30% FAT ZERO
 Curve C: 64-stage, 5.0 mil wide gates with no FAT ZERO

frequency for p-channel two-phase CCD's on (111) and (100) material using varying amounts of background charge or fat zero. The higher frequency capabilities of n-channel over p-channel CCD's are indicated in Figure 3.16. Three-phase, three-level polysilicon n-channel CCD's and two-phase offset mask p-channel CCD's have very good high frequency clock operation (Figure 3.17). As expected, the transfer inefficiency rises sharply when the time allowed for charge transfer is reduced to the order of the decay time constant.

To achieve superior performance at higher operating frequencies, bulk channel CCD's have been developed which utilize the larger fringing field contribution than is obtainable in surface channel CCD's. The effective capacitance C_{eff} (Eqs. 3.42, 3.43) is decreased because of the larger depletion region which increases the fringing field. The larger fringing field, in turn, decreases the single carrier transfer time. Figure 3.18 compares the channel potential profiles of SCCD's and BCCD's.

The fringing fields in BCCD's have been analyzed (numerically) for two-phase (15, 16, 22, 109), for three-phase (16, 22, 109), and for four-phase (112) structures using Poisson's equation and the depletion layer approximation. As for SCCD's, the minimum fringing fields occur at the center of the transfer well. The magnitude $\xi_{y_{min}}$ varies with the distance of the channel from the Si surface, and becomes a maximum for a depth of about 0.4L with a value

$$\xi_{f_{min \max}} \approx 0.5 \frac{\Delta V}{L} \quad (3.47)$$

provided that the total depletion region (on both sides of the well) is larger than about 2L. This value of $\xi_{f_{min}}$ can be inserted into Eq. 3.45 to calculate an approximate single carrier transfer time and to estimate the maximum frequency of operation for a bulk channel CCD.

Bulk channel devices are capable of high speed operation. A uniformly doped 4.5 μm thick epitaxial layer BCCD was measured to have

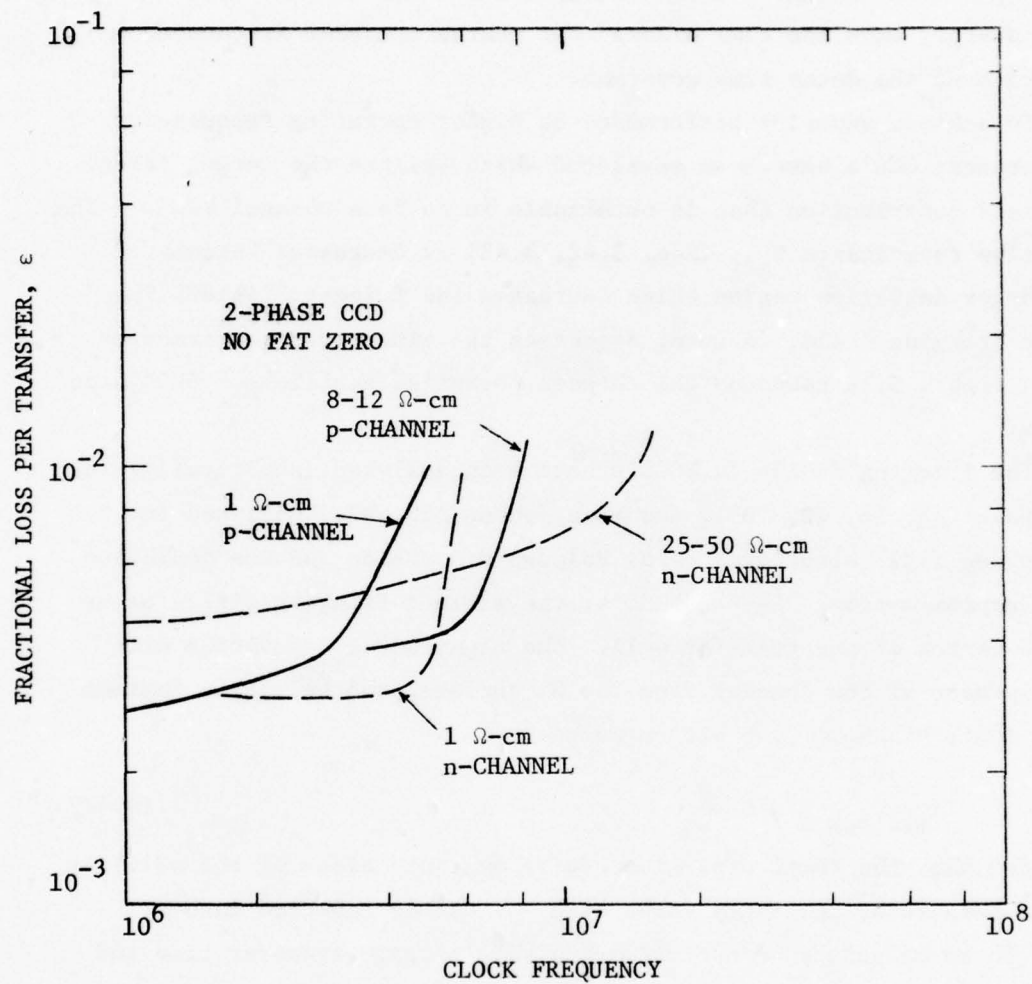
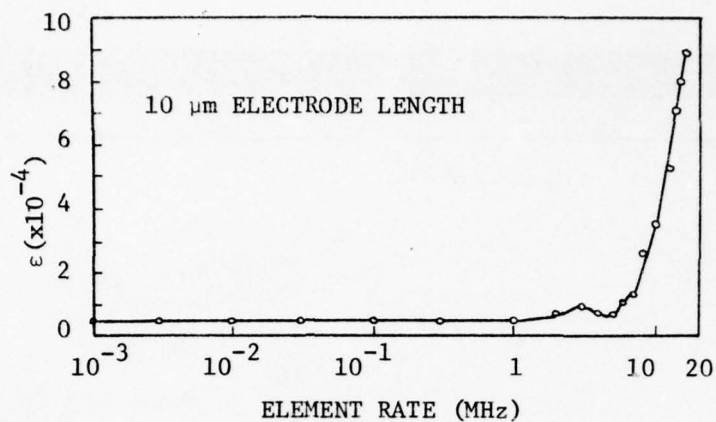
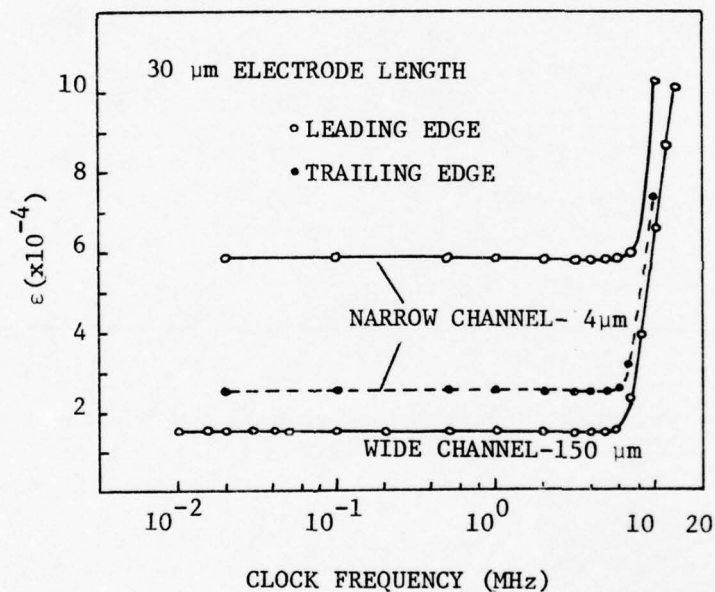


Figure 3.16. Comparison of n- and p-channel two-phase CCD transfer inefficiency versus clock frequency for (100) Si (after 113).



(a) Three-phase three-level polysilicon n-channel CCD (after 26).



(b) Two-phase offset mask p-channel CCD (after 9).

Figure 3.17. Transfer inefficiency as a function of clock frequency of two- and three-phase CCD's.

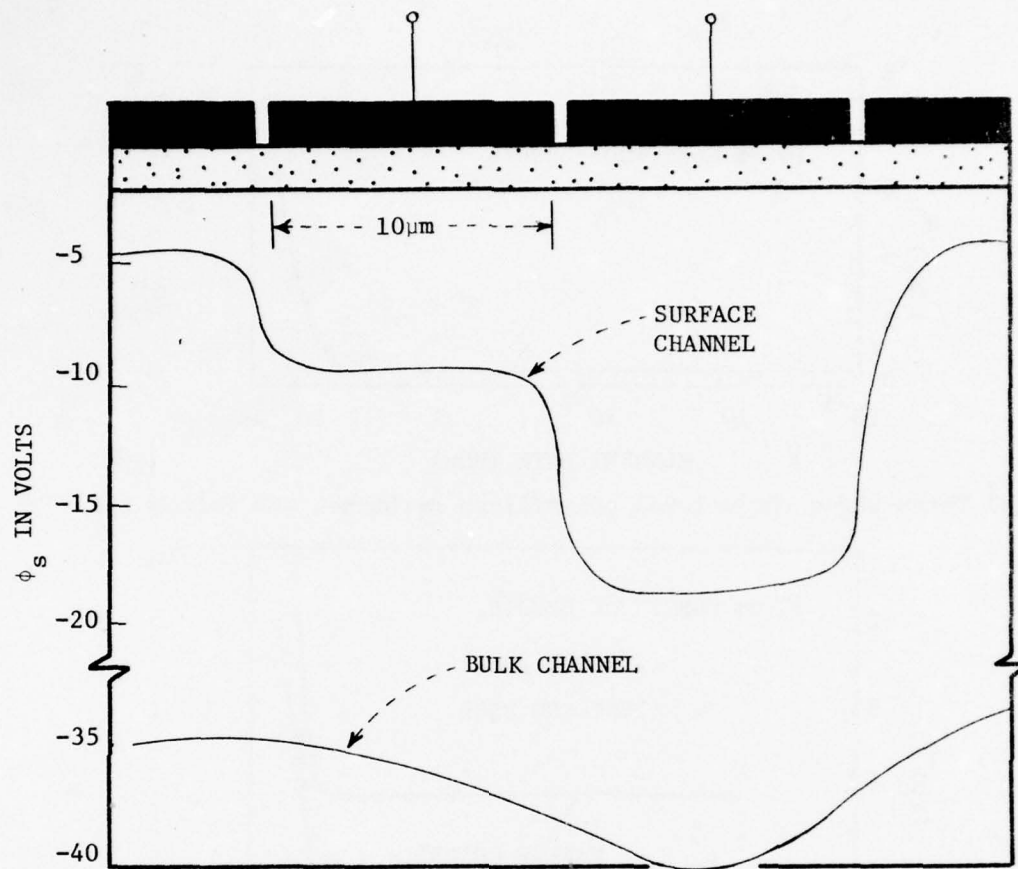


Figure 3.18. Potential profile along channel for p-channel SCCD and BCCD (after 91).

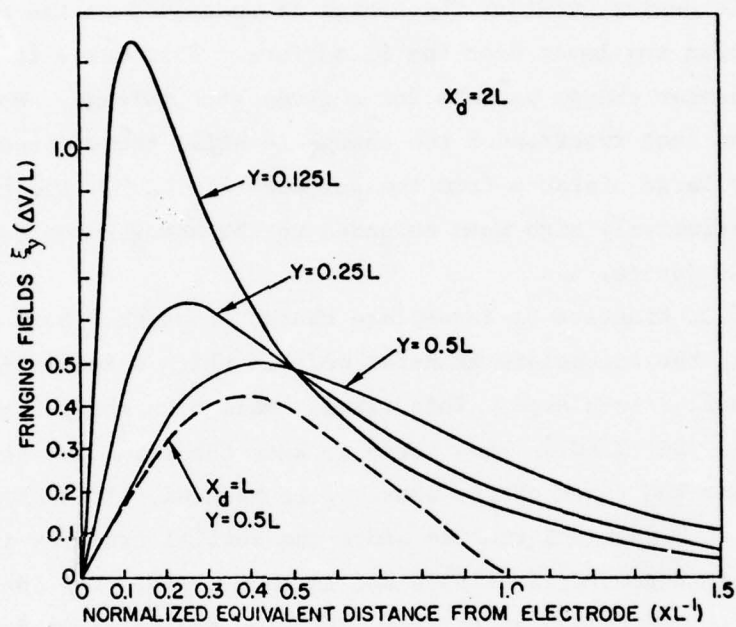
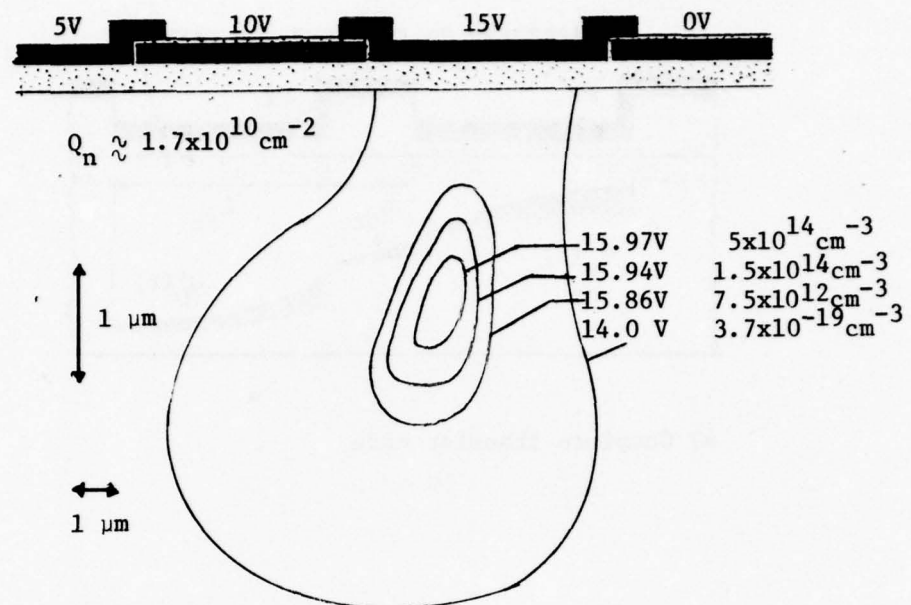


Figure 3.19. Normalized fringing fields E_y versus the normalized distance from metal-SiO₂ interface as a function of location under the electrode for bulk channel CCD's (after 112).

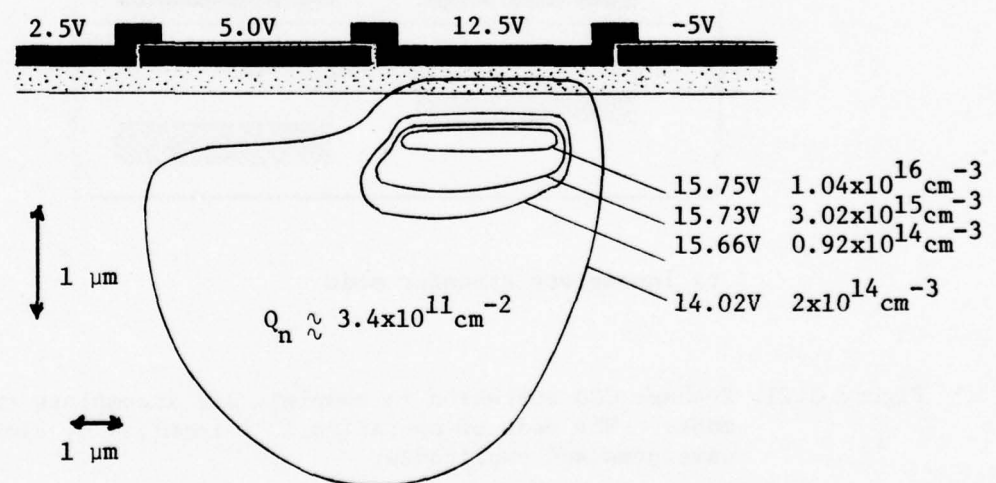
a transfer inefficiency of 5×10^{-5} at a 135 MHz clock frequency with 10V clock voltage changes (113) while profiled BCCD's have been measured at 135 MHz with transfer inefficiencies of the order of 1×10^{-4} . Figure 3.20 shows the equipotential and isoconcentration lines of a homogeneous doped, epitaxial layer, peristaltic CCD and a profiled peristaltic CCD. It should be noted that in the profiled peristaltic device, most of the charge is contained in the more heavily doped top layer near the Si surface. This makes it possible to store larger charge packets for a given gate voltage. However, because the last fraction of the charge is still transferred at a relatively large distance from the surface (Fig. 2.9), the transfer speed is relatively high when compared to the homogeneous doped peristaltic device.

3.2.3.2. Kinetics of incomplete charge transfer. Some CCD's are operated in the incomplete transfer mode in which a small bias charge is continually circulated. This fixed, small bias charge represents zero signal (FAT ZERO). This tends to keep the interface states saturated so that the fixed charge loss, δ , is reduced. It also permits operation at higher frequencies since the initial transfer is controlled by the self-induced drift fields and is thus rapid. The last 1% or so of charge is controlled by thermal diffusion and drift in fringing fields - relatively slow processes. Although the clock frequency can be used to control the bias charge, its magnitude must be well-controlled (particularly for analog applications) and in practice a potential barrier is used to control the FAT ZERO. Figure 3.21 shows a 2-phase CCD operation (a) in the complete transfer mode and (b) in the incomplete transfer mode. The effects of incomplete transfer of a 2-phase CCD are presented in Figure 3.22 for 0% and 10% FAT ZERO (30). Because operation in the incomplete transfer mode reduces the dynamic response and results in increased noise, the barrier heights, clock voltages, and clock frequencies are normally adjusted to produce as small a bias charge as practical.

3.2.3.3. Influence of clock waveforms. Not only does the clock

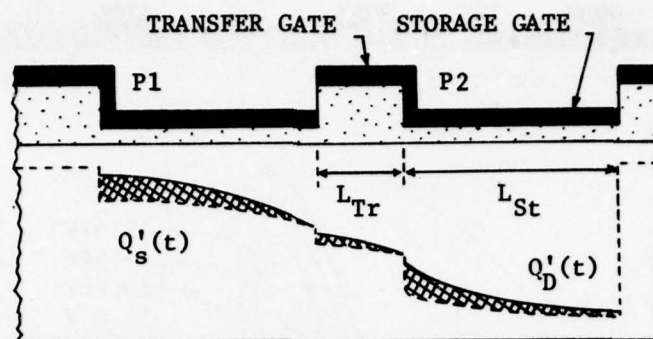


(a) Homogeneous n-layer: $N_D = 7.5 \times 10^{14} \text{ cm}^{-3}$, $d_n = 5.1 \text{ μm}$.

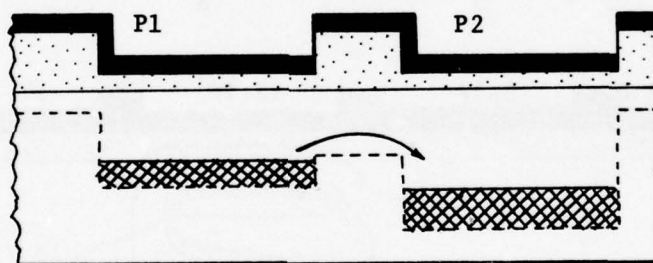


(b) Profiled n-layers: $1 \text{ μm n}^+ \text{ layer} - N_D (\text{surface}) = 2 \times 10^{16} \text{ cm}^{-3}$;
 $\text{n layer} - N_D = 2 \times 10^{14} \text{ cm}^{-3}$.

Figure 3.20. Equipotential and isoconcentration lines for various types of peristaltic devices (after 12).



a) Complete transfer mode



b) Incomplete transfer mode

Figure 3.21. 2-phase CCD operation in complete and incomplete transfer modes. The mode of operation is determined by clock waveforms and amplitudes.

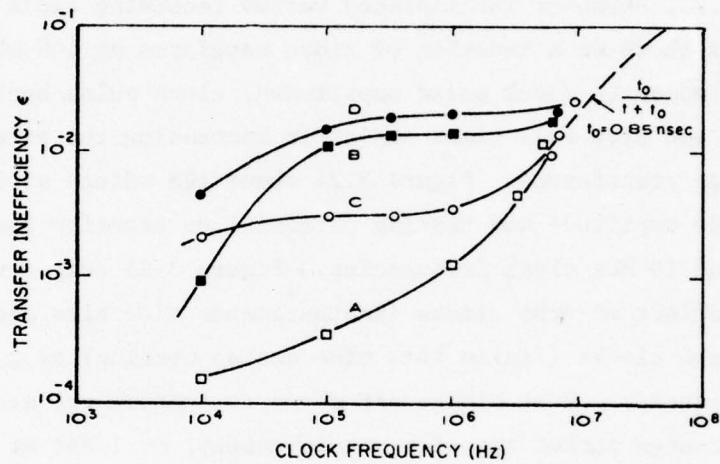
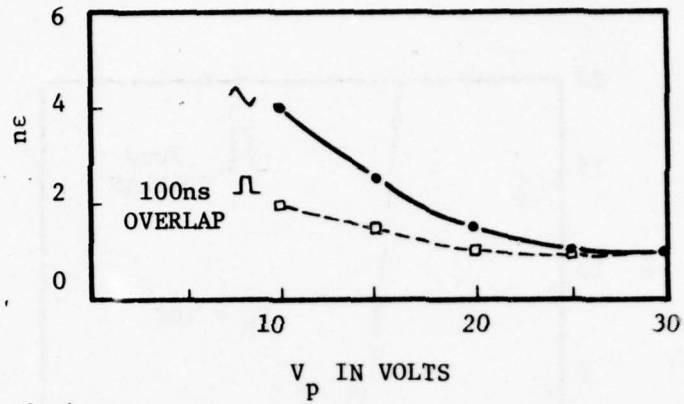


Figure 3.22. Transfer inefficiency versus clock frequency for 64-stage register on (100) substrates using incomplete transfer mode. Curves A and B represent operation at 10% FAT ZERO while C and D represent no FAT ZERO. Curves B and D represent operation with similar electrical drive and curves A and C represent operation at similar electrical drive but different from C and D (after 30).

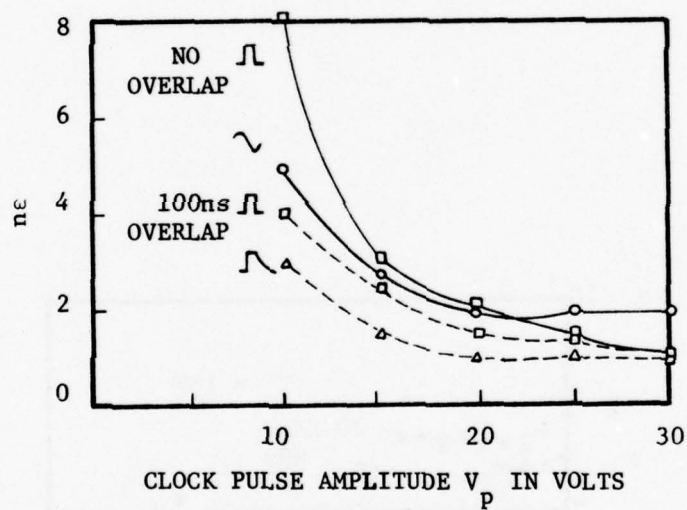
frequency affect the transfer inefficiency, but the clock waveform can also influence the charge transfer process.

If the potential under the sending electrode decreases too rapidly, the signal charge has insufficient time to transfer to the receiving electrode, and can be injected into the substrate as the inversion layer collapses, or can be transferred backward into the previous electrode (88, 108, 114, 115). To eliminate these problems, several techniques such as overlapping of clock pulses, non-rectangular waveforms, variation of clock pulse voltages, etc., have been employed. In Figure 3.23, transfer inefficiency versus receiving clock pulse amplitude is shown as a function of clock waveforms at 100 kHz and at 1 MHz. For moderate clock pulse amplitudes, clock pulse overlap is beneficial, and slow fall times assist in increasing the percentage of signal charge transferred. Figure 3.24 shows the effect of driving (clock) pulse amplitude and resting potential on transfer inefficiency for 1 MHz and 10 MHz clock frequencies. Figure 3.25 compares the calculated effect of drop clocks (instantaneous rise time and no overlap) with push clocks (finite rise time and no overlap) as a function of clock frequency. Push clocks are shown to improve the accuracy of the signal charge packet transfer significantly, at least at reasonable clock frequencies. Since, for actual CCD circuits, all waveforms have finite rise and fall times, clock pulse overlap has been investigated (86) in a more realistic situation (Figure 3.26). This investigation shows that at least 10 nanoseconds of pulse overlap is required to minimize the transfer inefficiency product.

3.2.3.4. Process related effects. Almost every process step variation can influence the transfer inefficiency of a CCD. However, there are some process and design variations which significantly change the CCD's ability to transfer charge efficiently. Two of these factors are substrate doping and electrode length. Substrate doping affects both the magnitude of the transfer inefficiency at low clock frequencies and the maximum acceptable clock frequency. In general, the low frequency transfer inefficiency factor decreases as the substrate doping concentration decreases. Thus, to minimize signal charge degradation

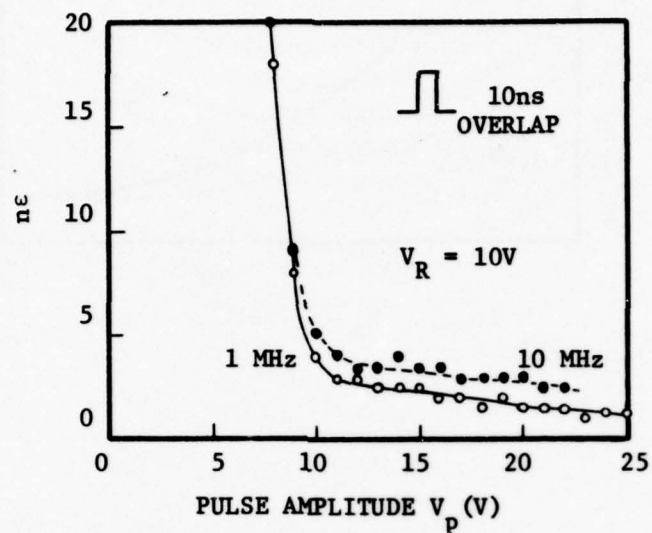


(a) 100 kHz clock rate.

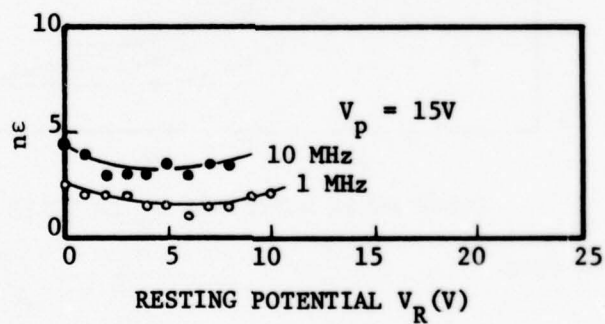


(b) 1 MHz clock rate.

Figure 3.23. Transfer inefficiency product versus clock pulse amplitude for various waveforms at 100 kHz and 1 MHz (after 86).



a)



b)

Figure 3.24. Transfer inefficiency product versus driving pulse amplitude (a) and resting potential (b) (after 86).

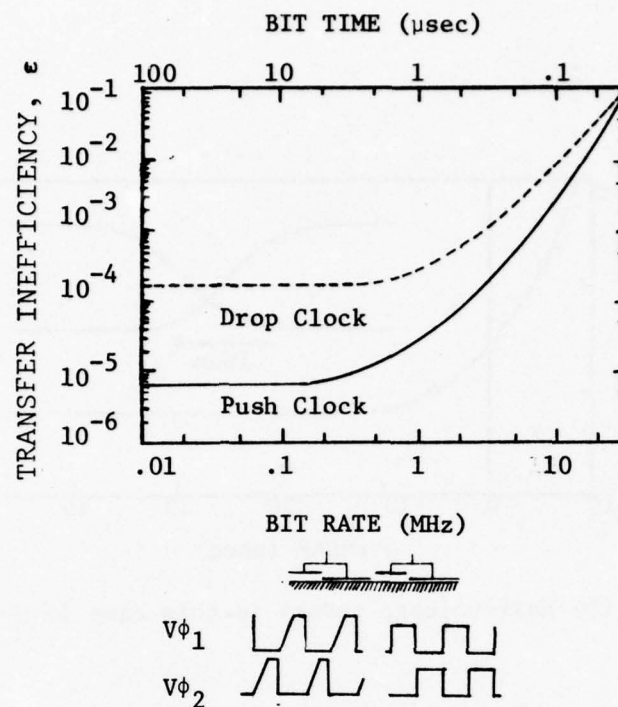
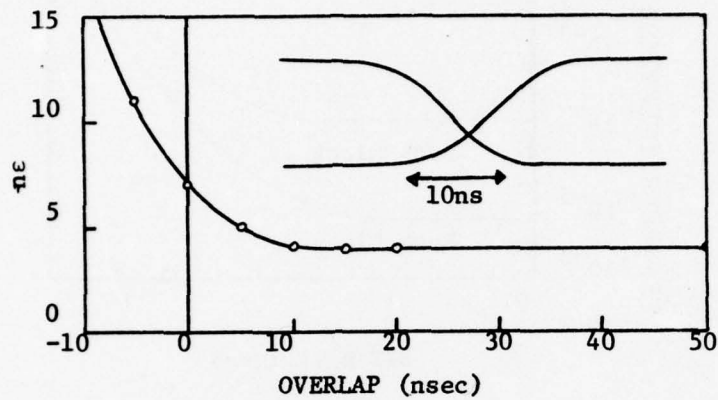
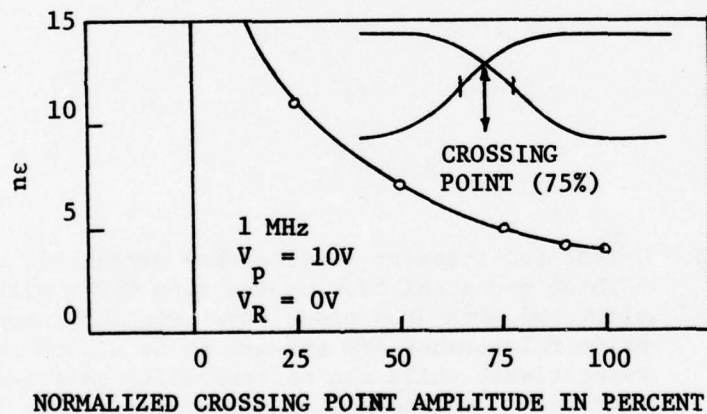


Figure 3.25. Calculated transfer inefficiency versus bit rate for 2-phase p-channel overlapping gate CCD's with push clock and with drop clock waveforms indicated. The oxide thicknesses are assumed to be $0.32\mu\text{m}$ and $0.12\mu\text{m}$ respectively while the corresponding gate lengths are taken as $0.8\mu\text{m}$ and $0.14\mu\text{m}$ respectively. In the push clocks a 13 nsec rise time is assumed (after 87).



a) Overlap (at the half-voltage point) in this case is negative.



b) Crossing point

Figure 3.26. Transfer inefficiency product versus clock pulse overlap (after 86). Specific examples are shown in the inserts.

at the expense of high frequency capability, high substrate doping concentrations (10^{15} to 10^{16} cm^{-3}) are used. If maximum frequency response is desired, the lowest possible substrate doping concentration (10^{13} to 10^{15} cm^{-3}) are used.

Figure 3.27a shows the minimum fringing field at the center of the electrode as a function of substrate doping concentration for p-channel 2-phase SCCD's indicating that low concentrations maximize the fringing fields and thus minimize the single carrier transfer time (Figure 3.27b). The maximum time is also limited by the thermal time constant, as indicated in Figure 3.28. It is noted that the length of the electrode controls the transfer efficiency and transfer speed. If the length of the electrode is decreased, the charge handling capability decreases but the single carrier transfer time also decreases because the fringing fields increase. Figure 3.29 illustrates this effect. Clearly, for high speed operation the electrodes should be as short as practical. However, it has been shown that interface state considerations limit the minimum length of the electrodes to about 5 μm (116). Table 3.2 lists transfer inefficiency at 1 MHz for n-channel and for p-channel SCCD's on (111) and (100) substrates with resistivity, orientation, and electrode length as parameters. The effects of oxide thickness, crystal orientation, and clock voltage on transfer inefficiency have also been calculated (106).

3.2.4. Charge trapping. At sufficiently low clock frequencies (below about 500 kHz), the transfer efficiency of a CCD which is operating in a complete transfer mode is no longer limited by free charge transfer effects but by charge trapping effects. When a charge packet is transferred to a potential well which has been empty for some time, empty trapping states under and around the new potential well trap some of the charge of the packet. These charges are emitted at some later time, depending on the emission time constant of the state. If the emission time is short enough for the charge to return to the well before the next transfer, the transfer efficiency is

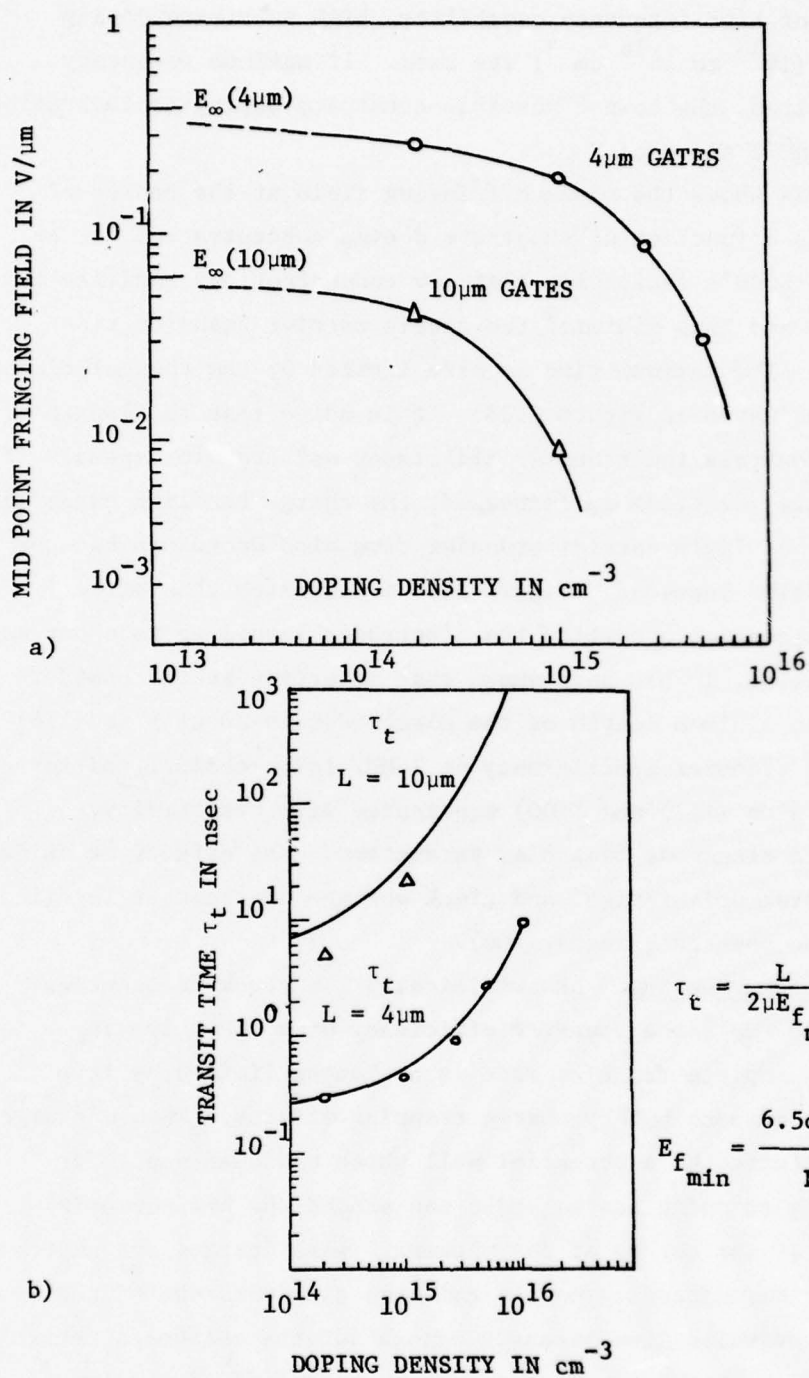


Figure 3.27. Effect of substrate doping concentrations on fringing fields (a) and single carrier transfer time (b) for 2-phase surface p-channel CCD's (after 100).

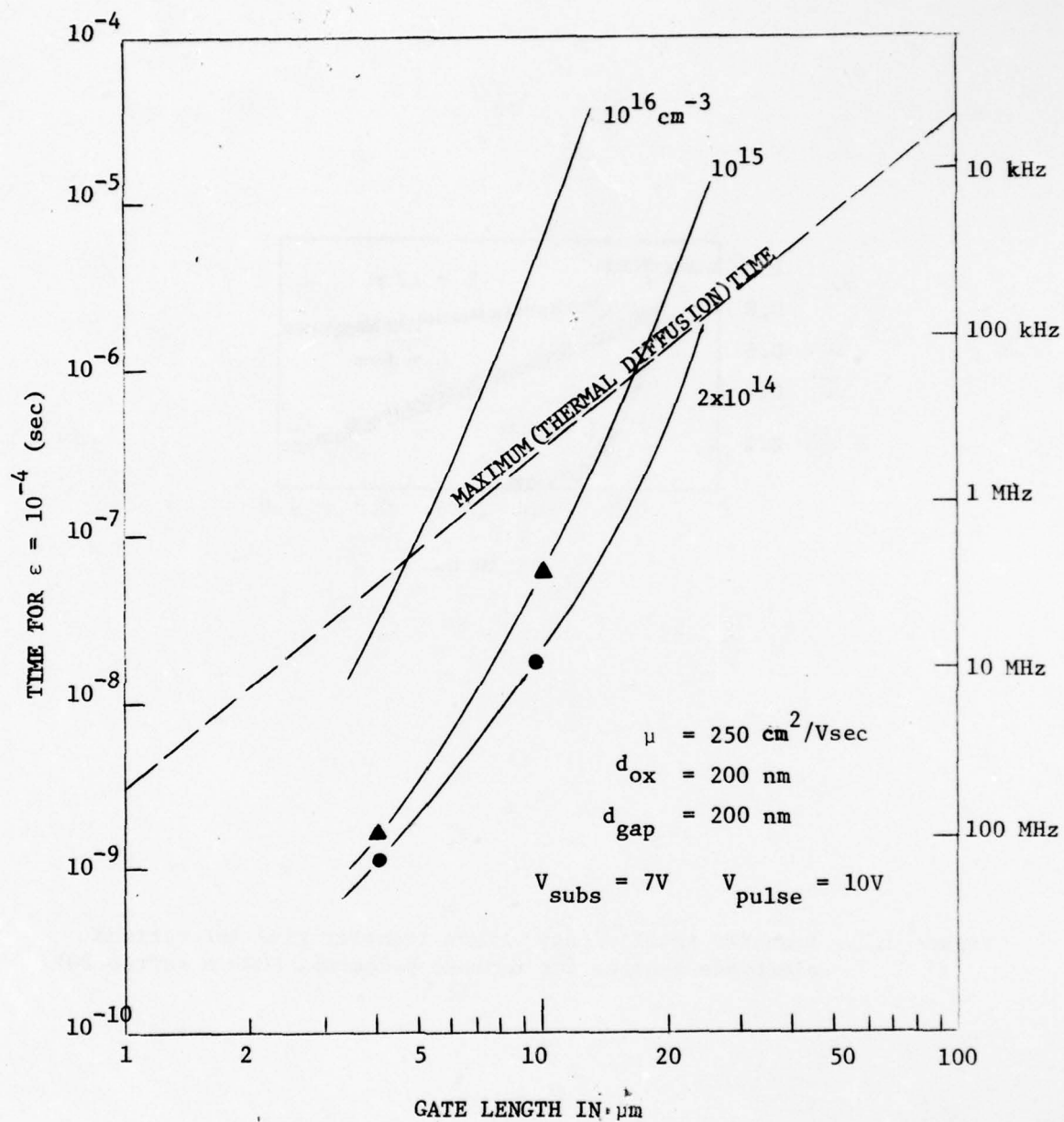


Figure 3.28. Time required to achieve $\epsilon = 10^{-4}$ versus electrode length as a function of substrate doping concentration for 2-phase p-channel SCCD (after 103).

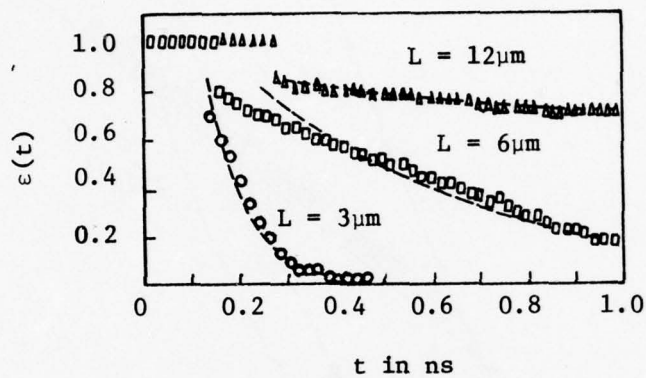


Figure 3.29. Transfer inefficiency versus transfer time for various electrode lengths for 3-phase p-channel SCCD's (after 20).

TABLE 3.2

Performance of the Tested Two-Phase CCD Registers
at 1.0 MHz Clock Frequency (after 113)

No.	Substrate			Channel Confinement	Channel Width [mil(μ m)]	Transfer Loss Per Gate With 20-30% Fat Zero	N_{ss} ($\text{cm}^{-2}\text{-eV}^{-1}$)
	Type	Resistivity (ohm-cm)	Orientation				
1	n	1.0	111	Thick Oxide	5.0(125)	1.2×10^{-4}	1.2×10^{11}
2	n	1.0	100	Thick Oxide	5.0(125)	5.0×10^{-5}	2.9×10^{10}
3	n	1.0	100	Thick Oxide	1.0(25)	1.0×10^{-4}	-
4	n	1.0	100	Thick Oxide	0.5(12.5)	3.5×10^{-4}	-
5	n	8-12	100	Diffusion Guard Ring	5.0(125)	2.0×10^{-4}	-
6	p	1.0	100	Thick Oxide	5.0(125)	$< 10^{-4}$	-
7	p	1.0	100	Thick Oxide	0.5(12.5)	2.0×10^{-4}	-
8	p	25-50	100	Poly-Si Field Shield	5.0(125)	3.0×10^{-4}	-
9	p	25-50	100	Poly-Si Field Shield	0.5(12.5)	1.2×10^{-3}	-
10	p	1.0	100	Poly-Si Field Shield	5.0(125)	1.2×10^{-4}	-
11	p	1.0	100	Poly-Si Field Shield	1.0(25)	2.5×10^{-4}	-
12	p	30	100	Poly-Si Field Shield	5.0(125)	1.8×10^{-4}	-
13	p	30	100	Poly-Si Field Shield	1.0(25)	4.0×10^{-4}	-

DEVICES 1 to 9 were 64- and 128-stage registers with 0.4 mil (10 μ m) polysilicon gates and 0.2 mil (5 μ m) aluminum gates.

DEVICES 10 to 13 were 500-stage registers with 0.3 mil (7.5 μ m) polysilicon gates and 0.1 mil (2.5 μ m) aluminum gates.

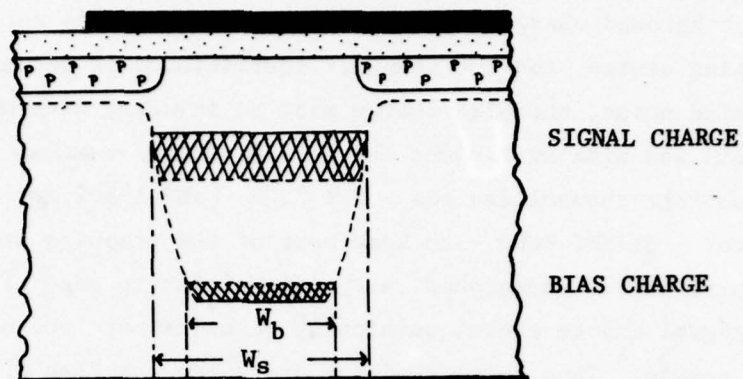
unaffected by the trap. However, if the emission time is long enough so that the charge is returned to the inversion region after the charge packet has been transferred, the charge is lost to the charge packet thereby increasing the transfer inefficiency of the CCD. Those carriers trapped in states having re-emission times comparable to, or longer than, the transfer time, will form a charge residual in the following packets. States with extremely long re-emission time constants are effectively constantly filled and do not affect the transfer inefficiency. Therefore, the interface states of importance are those with emission time constants $\tau_e \sim 1/mf_c$ where m is the number of phases. The kinetics of charge trapping and emission are described in terms of the Fermi-Dirac probability, modified for the case of non-equilibrium energy distribution of trapping states, and the details of the electron interaction with the interface states and with the conduction band. Phenomenologically, these are described by capture cross-sections of the states for trapping and emission time constants for re-emission. These parameters are quite process-dependent.

One of the main differences between surface channel and bulk channel CCD's concerns the type of traps which are predominant in each device. Surface channel CCD's have the charge packet confined within the first 100 nm from the interface, and thus are mainly concerned with silicon-silicon dioxide interface states located at or close to the actual interface. Since the charge packet of a surface charge CCD does not occupy significant silicon volume, charge trapping by bulk trapping states is not significant. For bulk channel CCD's, the charge packet is intentionally prevented from interacting with the interface states, and thus is trapped only by bulk silicon trapping states. However, the volume per unit charge in a bulk channel CCD is greater than in a surface channel device so that bulk trapping has a relatively larger effect.

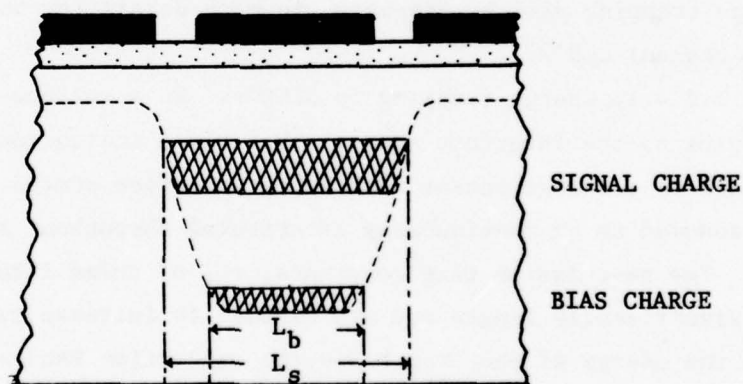
As indicated earlier, to diminish the effect of the trapping states, background charge or FAT ZERO is often introduced, especially in surface

channel devices, so that most of the trapping states remain filled by the background charge. The signal charge packet is not lost to empty trapping states, and the transfer inefficiency is decreased. To minimize noise, the bias charge must be injected with uniform charge packets and with sufficient charge (10 -50% of maximum charge capability) for surface channel devices - FAT ZERO - and 1-10% for bulk channel devices - SKINNY ZERO - to keep most of the trapping states full. However, use of background charge gives rise to edge effects because the signal charge packet physically occupies more volume than does the bias charge. Thus, some trapping states do not "see" the bias charge, and therefore trap charge from the signal charge packet. This is illustrated in Figure 3.30 for a SCCD. In (a) the hybrid diagram is shown on a cut across the potential well while (b) shows a cut parallel to the channel. The amount of surface area in contact with the bias charge is approximately $W_b L_b$, while that in contact with the signal charge is approximately $W_s L_s$. The difference, then, is effective in trapping signal charge. In the following sections, the problems of charge trapping will be discussed in more detail for both surface and bulk channel CCD's.

3.2.4.1. Charge trapping in SCCD's. In a surface channel CCD, trapping by the interface states takes place instantaneously upon the contact of a charge packet with empty interface states. These states are assumed to be continuously distributed throughout the energy band gap. The re-emission time constants, τ_e , of these interface states are significantly longer and are assumed to increase exponentially with the energy of the trap below the conduction band at the interface. The Shockley-Read model and rate equations are normally used to calculate trapping effects (10). Figure 3.31 is a schematic representation of the discharge of carriers from traps and the effective backward charge flow. Because the trapping states have exponential re-emission rates, with time constants dependent on energy below the

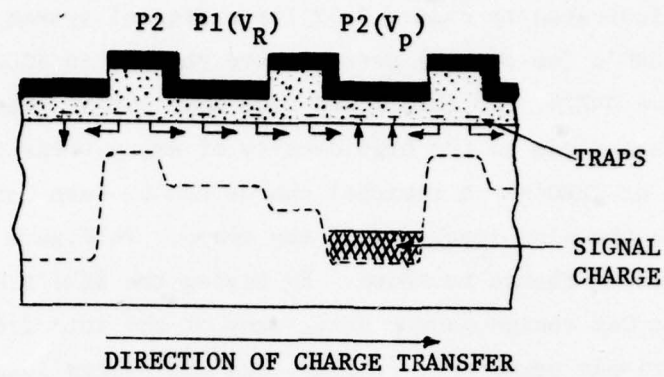


a) Transverse view indicating parallel edge regions

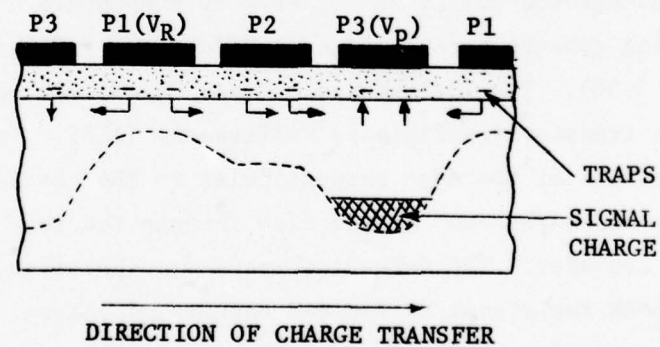


b) Longitudinal view indicating perpendicular edge regions

Figure 3.30. Hybrid diagrams of SCCD edge regions showing the difference in area exposed to bias charge and to signal charge (adapted from ref, 9).



a) Two-phase CCD



b) Three-phase CCD

Figure 3.31. Schematic representation of trapping and re-emission of signal charge by interface states (after 74).

conduction band, the shallow traps are emptied first while the charge in deeper traps require considerably more time to empty. This effect is illustrated in Figure 3.32 for a digital system in which a group of 160 ZERO's (no charge) were clocked through an SCCD before a sequence of five ONE's, two ZERO's and five more ONE's. The first ONE is highly attenuated due to the high density of empty traps following the long train of ZERO's. A residual charge can be seen behind the last ONE due to the slow discharge of the traps. In Figure 3.32b the effect of background charge is shown. By having the ZERO's represented by 10% of the ONE charge packet size, many of the interface states are effectively permanently filled, and the charge loss of the first ONE is significantly decreased. The residual charge after the last ONE is also somewhat reduced. The effect of the relative size of the FAT ZERO has been investigated for two-phase CCD's (30) and for three-phase CCD's (26) as shown in Fig. 3.33. It is seen that bias charge which is a significant fraction of the maximum handling capacity can decrease the transfer inefficiency of surface channel CCD's by as much as two orders of magnitude.

Background charge is not able to compensate completely for trapping centers because of edge effects as indicated earlier (Fig. 3.30). The "perpendicular" and "parallel" edges are found to affect transfer inefficiency differently (117). In the case of interface states at the edge perpendicular to the channel, the signal charge and background charge flow through the interface region during every transfer. The interface state can therefore capture carriers from both the signal charge and background charge. The trapping and re-emission of the carriers by these interface states is similar to that under transfer gates. For edge interface states parallel to the channel, clocking waveforms affect the transfer inefficiency of two-phase CCD's. Drop clocks affect the charge transfer by creating deeper potential wells under the next gates, and thereby preventing the background charge from reaching the parallel edge region. Thus,

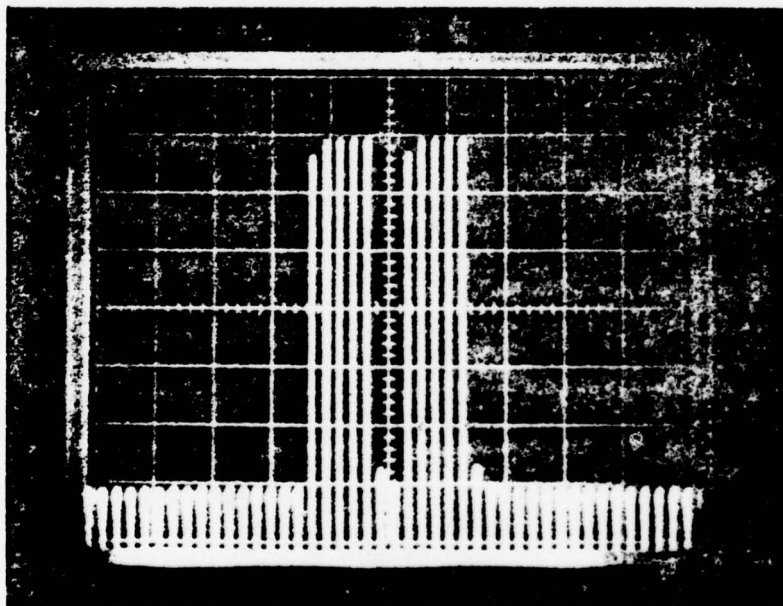
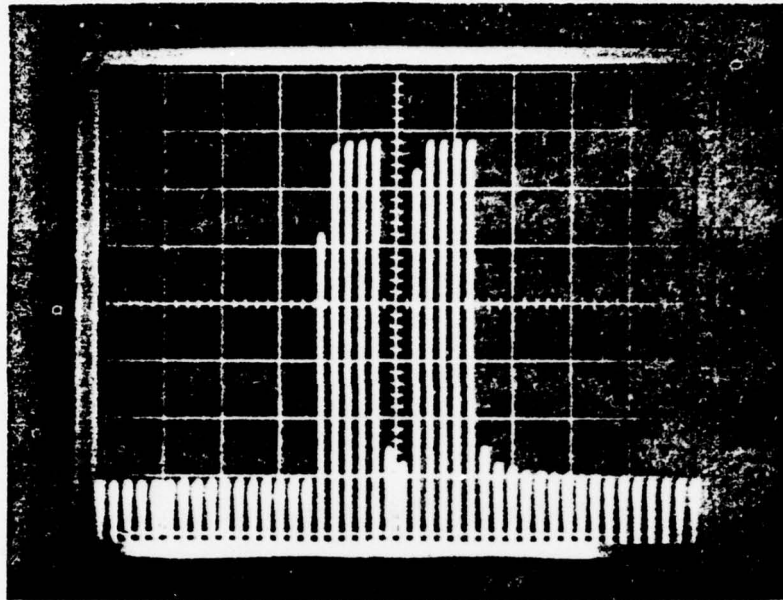


Figure 3.32. Output pulses of two groups of five ONE's separated by two ZERO's, after a string of 160 ZERO's for a 256 bit SCCD. Operation is shown at 1 MHz without background charge (top) and with 10% FAT ZERO (Bottom).

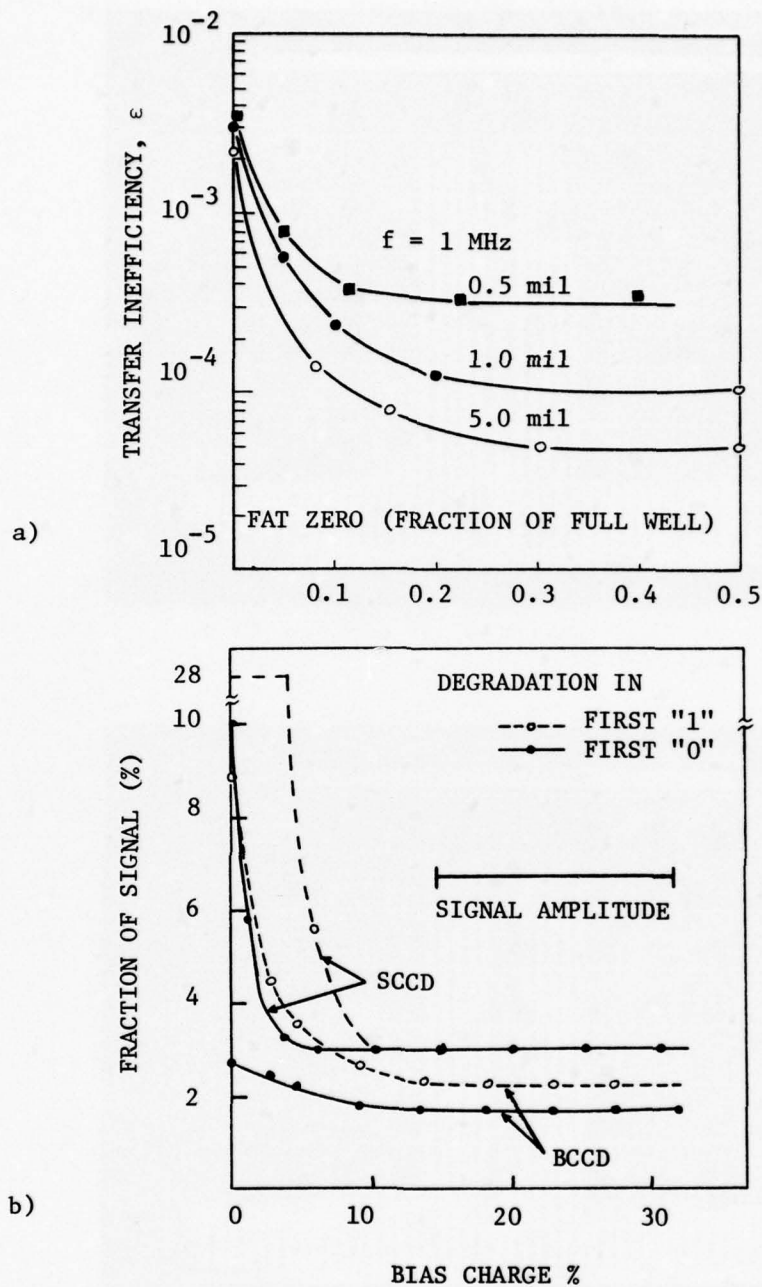


Figure 3.33. Effect of bias charge on signal degradation. In (a), the transfer inefficiency is shown for a 2-phase CCD with indicated channel widths (30) while in (b) the signal degradation is shown for a 256 element 3-phase SCCD's and BCCD's (after 26).

signal charge is trapped by the parallel edges, but background charge is not. Net charge trapped from the signal charge increases as the number of FAT ZEROS preceeding it increases, unlike all other charge trapping areas. The relative potential between the sending and receiving wells is not as great during the actual charge transfer with the use of push clocks and thus the FAT ZERO charge covers almost the same area as the signal charge and thus diminishes parallel edge effects.

Analyses have been made which assume that interface state density and capture cross-sections of the trapping state is independent of energy (118-120). However, it is thought that the interface state density increases monotonically and the capture cross-section of the traps decreases very rapidly as the energy approaches the energy band edges (121). A detailed analysis is difficult since the actual variation of capture cross-section and interface state density with energy is not well understood. Using the constant cross-section and density approximations, it is possible to develop simple expressions which give a rough idea of the effect of interface states on transfer inefficiency. For zero background charge the transfer inefficiency can be approximated by (119)

$$\epsilon = \frac{qkTN_{ss}}{C_{ox}\Delta\phi_s} \ln(p+1) \quad (3.48)$$

where N_{ss} is the interface state density, $\Delta\phi_s$ is the change in the interface potential due to the signal charge, and p is the number of phases. This case describes the amount of charge emitted into the first ZERO following a series of ONE's. To take into account the effect of bias charge, the transfer inefficiency is given by

$$\epsilon_b = \gamma \frac{qkTN_{ss}}{C_{ox}\Delta\phi_s} \ln(p+1) \quad (3.49)$$

where

$$\gamma = 1 - A_b/A_s \quad (3.50)$$

and A_s is the area occupied by the signal packet, and A_b is the area occupied by the background charge. Of obvious importance in minimizing the interface state contribution to transfer inefficiency is the requirement to keep N_{ss} as low as possible. Typical interface state densities calculated from measured transfer inefficiencies are approximately $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ for (111) orientation and 2×10^{10} to a low of $1 \times 10^9 \text{ cm}^{-2} \text{ eV}^{-1}$ for (100) orientation (26, 30).

3.2.4.2. Charge trapping in BCCD's. Bulk channel CCD's are designed to eliminate interface trapping problems and thus show similar but smaller charge trapping effects than surface channel devices (18). The bulk silicon trapping states are then important. They are assumed to be described by discrete energy levels in the energy band-gap and to obey the Shockley-Read-Hall model. Using various assumptions, an equation has been derived (122) which gives the amount of trapped charge emitted into the first trailing empty well after a string of charge packets,

$$\Delta Q' = qN_t V_s' e^{-1/mf_c \tau_e} [1 - e^{-1/f_c \tau_e}] \quad (3.51)$$

where N_t is the concentration of bulk traps, and V_s' is the volume occupied by the signal charge. An example of the attenuation of the first ONE and the charge residual in the first ZERO is shown in Figure 3.34 with 0% and 10% FAT ZERO. Comparing this figure with Fig. 3.32 for an equivalent surface channel device, a lesser first ONE attenuation and a lesser first ZERO charge residual are evident for bulk channel devices.

In general, the performance of bulk channel CCD's is less affected by trapping than an equivalent surface channel CCD because of the relatively low density of bulk trapping states. Bulk channel CCD's show significantly less signal degradation, particularly in the absence of background charge. Figure 3.33 shows that the improvement of the first ZERO with background charge is slight while somewhat greater improvement is seen in the first ONE with increasing FAT ZERO.

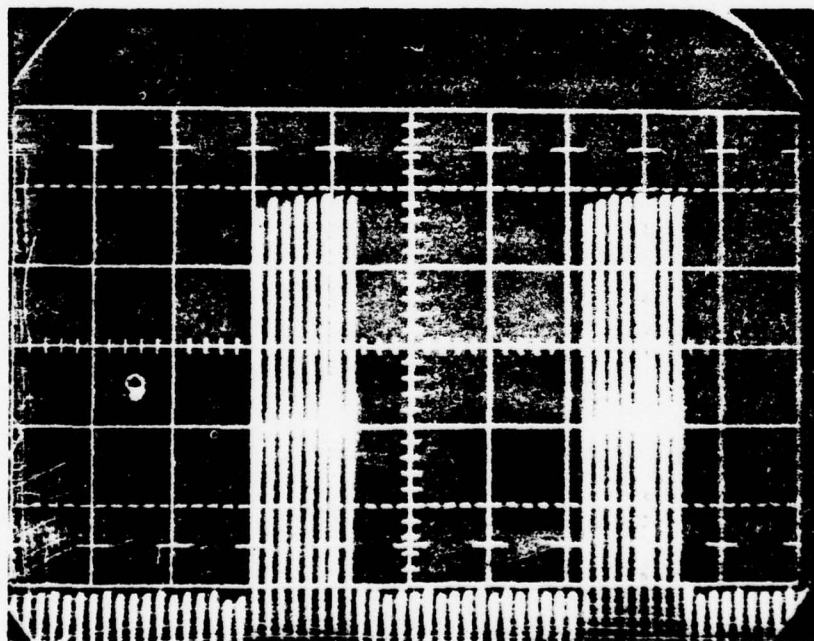
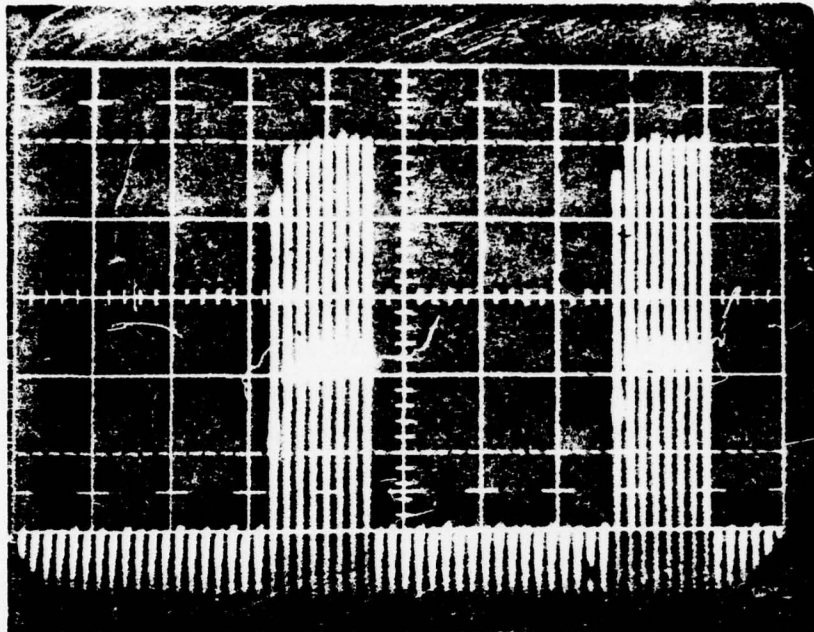


Figure 3.34. Output pulses of two groups of eight ONE's after a string of 4062 ZERO's for a 256 bit BCCD. Operation is shown at 6 MHz without background charge (top) and with 10% FAT ZERO (bottom).

Transfer efficiency in bulk channel devices is limited at sufficiently low clock frequencies by volume edge effects, similar to the surface edge effects discussed for surface channel devices. The volume which the charge packet occupies varies strongly with the size of the charge packet (Fig. 2.9) and thus the use of background charge results in a much smaller relative improvement than in surface channel devices. In Figure 3.35, the theoretical spatial extent of the charge packet and the charge loss on the first ONE is plotted as a function of charge packet size.

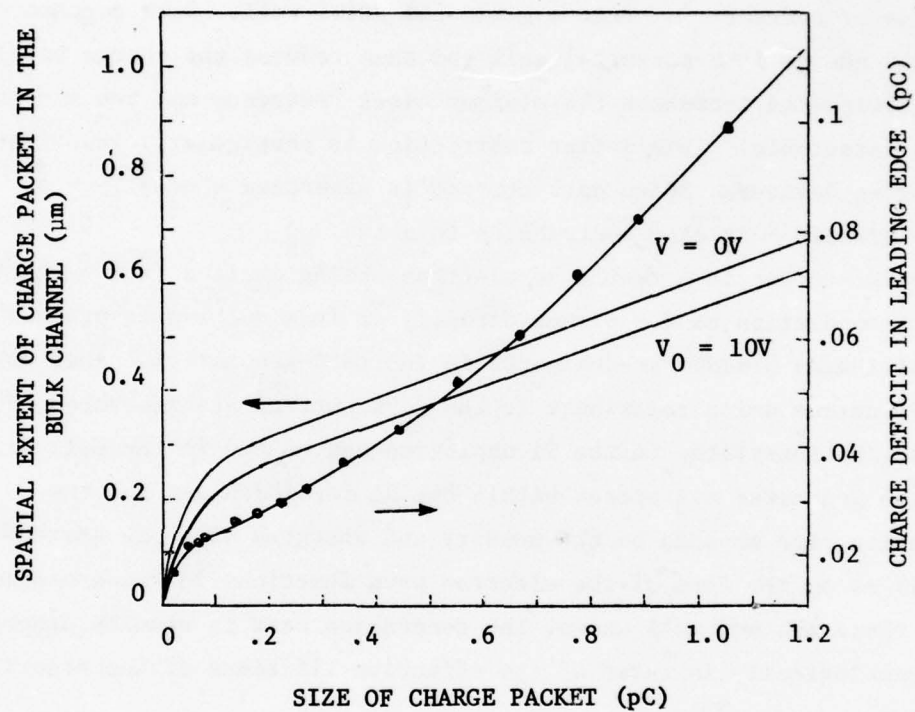


Figure 3.35. Calculated spectral extent of charge packet and measured charge loss in first ONE as function of charge packet size for bulk channel CCD (after 18).

3.3. Dark Current

Dark current refers to the output of a CCD in the absence of charge injection - either electrical injection at the input gate or optical injection in the interior of the CCD. It is convenient to discuss this in terms of current into a given potential well. Dark current produces charge in a potential well and thus reduces the charge handling capabilities and increases the minimum clock frequency and the minimum signal detectable. This latter restriction is particularly important in imaging devices. Since dark current is generated thermally - a random process - it also contributes to noise.

Dark current is a result of electrons being excited from valence band to conduction band - either directly or in a multi-step process. The multi-step process predominates in indirect-gap material such as Si. Electrons which contribute to the dark current are generated at the SiO₂/Si interface, in the Si depletion region and in the bulk Si. They are generated via states within the Si forbidden gap and the generation rate depends on the density and energies of these states as well as on the form of the electron wave functions in these states. Since these are not well known, the generation rate is usually described phenomenologically in terms of the effective lifetimes of the minority carriers.

Gross defects such as precipitates can result in localized regions with extremely short lifetimes. If such a defect should occur within a diffusion length of a given potential well, that well will be filled almost instantaneously. Such a "spike" makes the CCD unusable.

Electrons (in a p-type substrate) which are generated within a diffusion length of the depletion region contribute to dark current. The generation rate for this process is

$$g = \frac{n_p}{\tau_n} \quad (3.52)$$

where n_p is the equilibrium electron density in the p-type Si, and τ_n is the electron lifetime in this region and depends on the defect

concentration. Since $n_p = N_i^2/N_A$ where N_i is the electron concentration in intrinsic Si and N_A is the net acceptor concentration,

$$g = \frac{N_i^2}{N_A \tau_n} \quad (3.53)$$

The dark current density J_{nd} flowing into a potential well from the bulk Si is then

$$J_{nb} = \frac{q N_i^2 L_n}{N_A \tau_n} \quad (3.54)$$

Si can be regularly produced with τ_n large enough so that this contribution to dark current is normally negligible in comparison to other sources. Electron generation at the Si surface via interface states and in the depletion region via trap states are major sources of dark currents. Carriers generated within the depletion region are normally considered to obey the Sah-Noyce-Schockley model where the generation rate is

$$g = \frac{N_i}{2\tau_n} \quad (3.55)$$

where τ_n now represents the electron lifetime in the depletion region and is inversely proportional to the trap concentration. The current density flowing into a well from electron generation in the depletion region is then

$$J_g = \frac{N_i X_d}{2\tau_n} \quad (3.56)$$

Since the depletion width, X_d , is a function of the charge in the well, the dark current decreases with increasing signal charge at a fixed gate voltage.

The carrier generation rate at the interface depends on the number and characteristics of the interface states as well as their occupancy. This contributes to the dark current then, is time dependent and is a function of past history. It can be reduced by the use of a FAT ZERO.

To reduce the dark current the interface state and bulk trap state densities must be reduced. The densities of these states depend on the starting material and on processing conditions and thus can vary widely from manufacturer to manufacturer, from wafer lot to wafer lot and even from wafer to wafer within a lot. As discussed in chapter 2, numerous process steps have been devised to minimize these effects. These include HCl oxidations, heavy ion implantation on the backside of the wafers, phosphorus gettering processes. For impurities such as copper, iron, gold, etc., which segregate out at lattice dislocations, processes have been developed to reduce the dislocation densities. These include low temperature processing, and slower pull rates from high temperature furnaces. Another technique is to create a high dislocation density on the wafer backside near the end of the processing to attract the segregated impurities to the backside and away from the active surface. Even with all of these techniques, dark currents at room temperature can range from as low as 5 nA/cm^2 to as high as several hundreds of nA/cm^2 . In addition, the dark currents are rarely uniform and create pattern noise in CCD's.

3.4. Noise

A limitation of CCD's results from the degradation by noise of the information contained in the charge packets. Noise consists of a non-predictable variation of the voltage output. Except for that noise generated in the detection circuits, the output noise power is proportional to the variance of the charge in the packet being detected. It is thus convenient to discuss noise in CCD's in terms of the variance in the number of electrons, or in the charge, of a given well

$$\overline{(\Delta n')^2} = \overline{(n' - n'_{ave})^2} \quad (3.57a)$$

$$\overline{(\Delta Q'_n)^2} = \overline{(Q'_n - Q'_{n ave})^2} \quad (3.57b)$$

Since each capacitor is charged through a finite resistance, the stored charge is a function of the Nyquist or Johnson noise associated with that resistance. Consider the circuit of Fig. 3.36a. The Norton equivalent circuit is shown in Fig. 3.36b where the equivalent noise current generated in the frequency range df is given by $i_n = \sqrt{\overline{i_n^2}}$ where

$$\overline{i_n^2} = \frac{4kT}{R} df \quad (3.58)$$

The noise voltage on the capacitor in the range df is then

$$v_n = i_n |Z| \quad (3.59)$$

$$\text{where } |Z| = \frac{R}{\sqrt{1 + \omega^2 R^2 C'^2}} \quad (3.60)$$

over the total frequency range

$$\overline{v_n^2} = \int_0^\infty \frac{4kT}{R} \left(\frac{R^2}{1 + \omega^2 R^2 C'^2} \right) \frac{d\omega}{2\pi} \quad (3.61)$$

which integrates to

$$\overline{v_n^2} = \frac{kT}{C'} \quad (3.62)$$

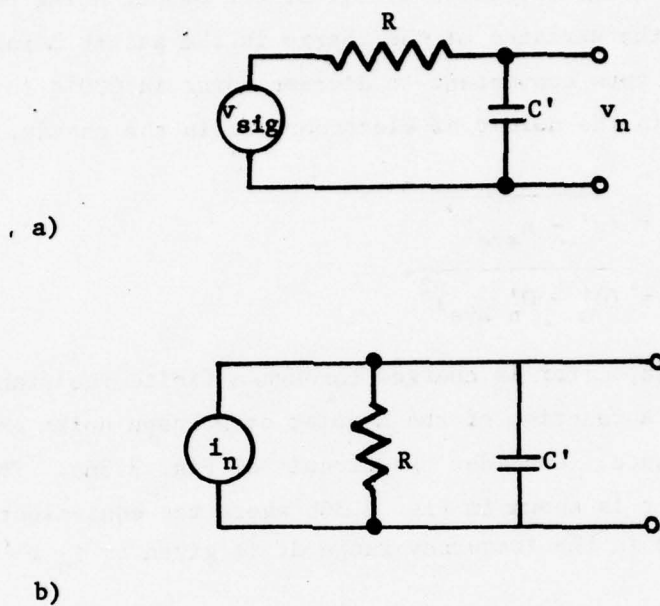


Figure 3.36. Capacitor charging circuit (a), and Norton noise equivalent circuit (b). The noise source is represented by an equivalent noise current $i_n = \sqrt{i_n^2}$

Since

$$\Delta Q'_n = C'_n v_n \quad (3.63)$$

$$\Delta Q'_n = kTC' \quad (3.64)$$

and

$$\Delta n' = \frac{1}{q} \sqrt{kTC'} \quad (3.65)$$

At room temperature

$$\Delta n' \approx 400 \sqrt{C'_{pf}} \quad (3.66)$$

where C'_{pf} is the capacitance in picofarads.

In addition to this basic noise associated with each capacitance, noise is generated by fluctuations in the input signal - either electrical or optical - , fluctuation in dark current, and fluctuation in transfer efficiency. There is also noise associated with signal detection and amplification (125). These noise sources are illustrated schematically in Figure 3.37.

3.4.1. Electrical injection noise. Electrical injection noise results from a fluctuation in the size of the injected charge packet for a given signal input voltage. In addition to the capacitance noise just discussed, there is shot noise present since the charge is usually injected over a potential barrier. Excess noise is also introduced. Its magnitude depends on the method used to inject charge (Section 2.5.1, Figure 2.25). For the dynamic current injection method, imperfect control of the pulse width causes noise in addition to the noise resulting from the fluctuations in voltage levels and the charge source. In the gate cutoff method, the inaccuracy of the gate voltage pulse and the division of charge under the gate electrode during turn-off between the diode and first potential well creates noise. Using the various potential equilibration methods, thermal fluctuations of the charge retained in the metering well with capacitance C'_M should be between

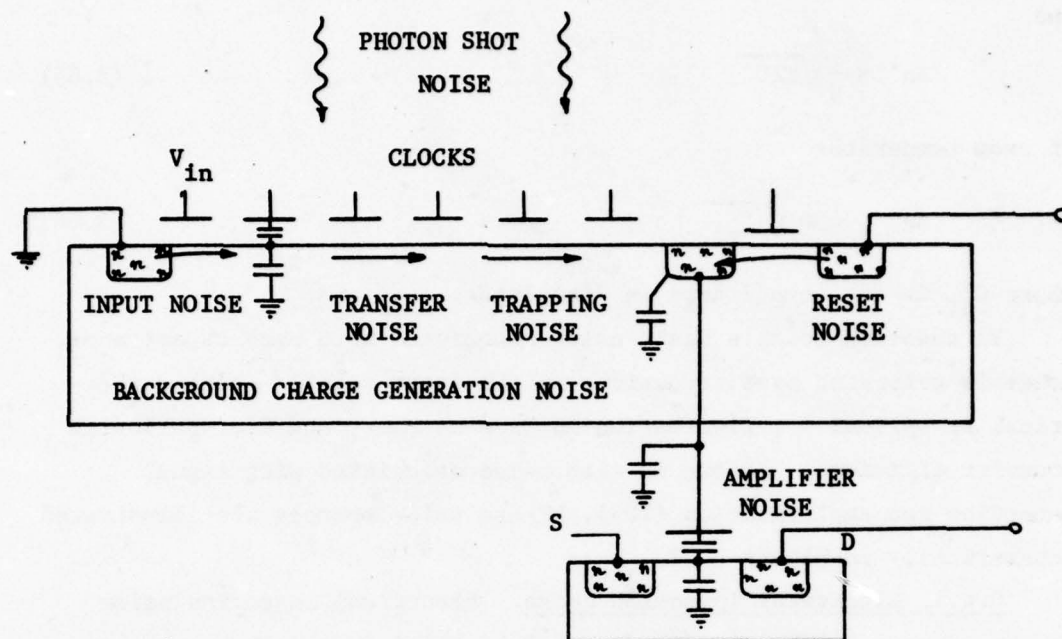


Figure 3.37. Schematic representation of various noise sources in a CCD (after 125).

$2kTC_M'/3$ and $kTC_M'/2$ depending on the time for equilibration. Fluctuations due to voltage pulses can be eliminated by holding $G1$ at a constant voltage. Figure 3.38 shows experimental data of the improved potential equilibration method.

3.4.2. Generation noise. Because electron generation resulting in dark current is a random process, it contributes to noise. This is shot noise and the considerations of shot noise apply. If there are n_d' (dark) electrons generated in a given well the variance in n_d' is

$$\overline{(\Delta n_d')^2} = n_d' \quad (3.67)$$

or the variance in the charge in the packet is then

$$\overline{(\Delta Q_d')^2} = qQ_d' \quad (3.68)$$

Since the variance is additive, the generation noise at the output of a register of n stages is

$$\overline{(\Delta Q_d')^2}_n = q \sum_{i=1}^n Q_{di}' \quad (3.69)$$

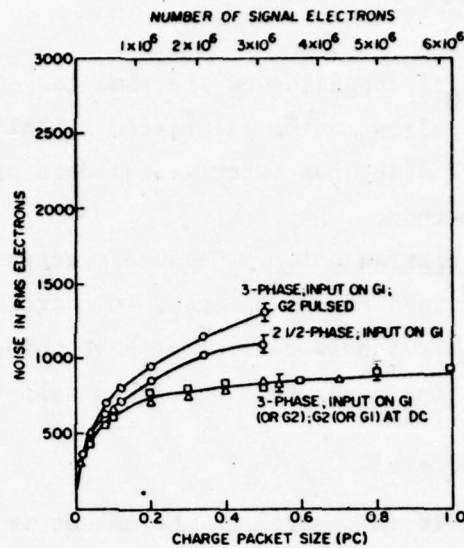
where Q_{di}' is the dark charge generated in the i 'th well.

Since Q_{di}' increases with time, so does the generation noise. Thus, devices such as imagers with long integration times, and cyclic shift registers for use in large memory arrays are extremely sensitive to this type of noise and their limits of operation are determined by the generation rate of dark current. To decrease this dark current noise, imagers are sometimes cooled.

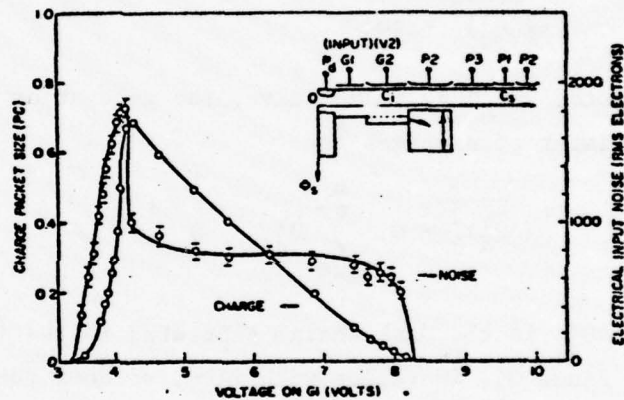
In an imaging device, the arrival of photons is a random process and so shot noise is associated with the signal. Letting n_{sig}' and Q_{sig}' represent the number of signal electrons and the signal charge in a given well, respectively, as for dark current noise,

$$\overline{(\Delta n_{sig}')^2} = n_{sig}' \quad (3.70a)$$

- a) Input noise of various injection methods.



- b) Input noise and charge packet size with signal on G1 and 8.3V on G2.



- c) Input noise and charge packet size with signal on G2 and 4.5V on G1.

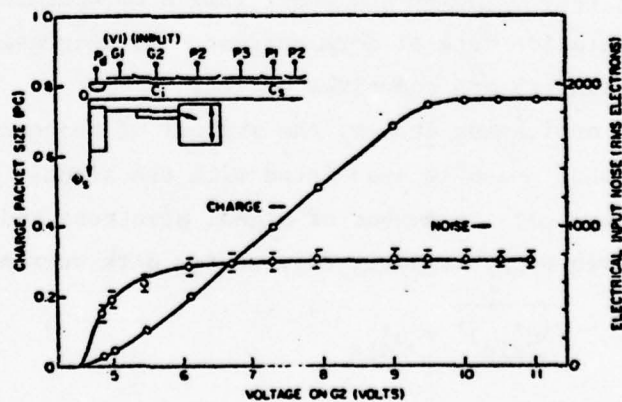


Figure 3.38. Input noise for improved potential equilibration method (after 127)

$$\overline{(\Delta Q'_{sig})^2} = q Q'_{sig} \quad (3.70b)$$

$$\overline{(\Delta Q'_{sig})^2}_n = q \sum_{i=1}^n Q'_{sig i} \quad (3.71)$$

3.4.3. Transfer noise. There are several noise mechanisms involved with transferring charge along a shift register. These involve the inherent noise associated with charging a capacitor, noise due to incomplete charge transfer, and noise involving trapping and emission from interface states and from bulk trap states.

During each charge packet transfer, some charge is left behind. If this amount could be controlled exactly, the transfer would be noiseless, but the remnant charge depends on signal size as well as device parameters, and exhibits random fluctuations, thus introducing noise. A correlation exists between adjacent charge packets because charge lost from one packet is picked up by following charge packets. Individual charge packets therefore have two fluctuations in size because of loss of charge to following packets and pickup of charge from preceding packets. The spectral densities of transfer and storage noise have been calculated. Assuming that the fluctuations in each transfer are independent, neglecting incomplete transfer effects, and assuming frequencies limited to below the Nyquist limit of $f_c/2$, the following equations were derived for transfer noise spectral density (116)

$$S_{tr}(f) = 4n \frac{\overline{\Delta Q'_{tr}{}^2} f_c}{q} (1 - \cos 2\pi f/f_c) \quad (3.72)$$

and for storage noise spectral density

$$S_{st}(f) = 2n \frac{\overline{\Delta Q'_{st}}}{q} f_c \quad (3.73)$$

where n is the number of transfers and $\overline{\Delta Q_{tr}^2}$ and $\overline{\Delta Q_{st}^2}$ are the mean square fluctuations in the transfer and storage charge packets respectively. While the storage noise spectral density is constant with frequency as expected, the transfer noise spectral density is suppressed for low frequencies and enhanced for high frequencies.

If n is not much less than 1, or in the case of significant transfer inefficiency, there is an intermixing of the charge packets and their noise as they move through the CCD. This has been shown (123, 124) to lead to a reduction in the noise components. The noise produced during the end of the transfer cycle is the least suppressed and thus the most important. From this overall view, there are several sources of transfer noise which will be discussed in more detail.

3.4.3.1. Incomplete transfer noise. In C4D's and other two-phase process-induced barrier CCD's operation in an incomplete transfer mode where part of the charge packet is left behind because of a potential barrier is possible. Variations in the channel conductance, emission of carriers across the barrier and direct feedthrough of clock noise have been considered (123, 124). Using a MOSFET model, the transfer noise fluctuations are given by

$$\overline{\Delta Q_{tr}^2} = \frac{2}{3} kTC'_s \quad (3.74a)$$

for charge retained on the source (where C'_s is the source capacitance) or

$$\overline{\Delta Q_{tr}^2} = \frac{1}{2} kTC'_s \quad (3.74b)$$

in the final stages of transfer where the discharge process becomes emission limited. The frequency of operation determines which equation is valid. Estimating the effect of clock variations,

$$\overline{\Delta Q_{cl}^2} = \overline{\Delta V_{cl}^2} C_{gs}^2 \quad (3.75)$$

where C'_{gs} is the gate-to-source capacitance.

3.4.3.2. Interface state noise. For surface channel devices (and some bulk channel devices with relatively large charge packets) functioning in the complete charge transfer mode, the dominant noise source is the fluctuation in the occupancy of the interface states or traps (119, 125). It is shown that only those states with re-emission time constants on the order of the transfer time contribute significantly to the noise. Assuming the usual exponential relation between the emission probability, and integrating over all possible energy levels

$$\overline{\Delta Q'^2_{ss}} = q^2 k T A_s N_{ss} \ln 2 \quad (3.76)$$

where A_s is the area of the electrode under which the interface states are filled and the interface state density, N_{ss} , is assumed to be constant with respect to energy. The expression is time or frequency independent if the density of states is assumed to be continuous with energy. Using this expression, a signal-to-noise power ratio for each individual charge packet can be obtained (9)

$$S/N = \frac{A_s C_{ox}^2 V_{sig}^2}{2 n k T N_{ss} \ln 2} \quad (3.77)$$

Combining equation 3.76 with Eq. 3.72, the noise power spectrum for properly filtered signals is

$$S(f) = \frac{4 k T \ln 2}{q} n f_c A_s N_{ss} (1 - \cos 2 \pi f / f_c) \quad (3.78)$$

This expression has been verified experimentally (57, 126, 127) and interface state densities of $1 \times 10^9 \text{ cm}^{-2} \text{ eV}^{-1}$ were estimated for an overlapping 3-phase electrode, (100), n-channel CCD. Figure 3.39 illustrates the spectral distribution of transfer noise measured on this device at 1 MHz.

3.4.3.3. Bulk trap noise. For bulk channel devices, the bulk traps introduce transfer noise. Since the trap levels are assumed to be discrete, the noise associated with the k 'th level should be frequency dependent and peak at frequencies on the order of the reciprocal of the emission time constant τ_{bk} . Summing over all discrete trap

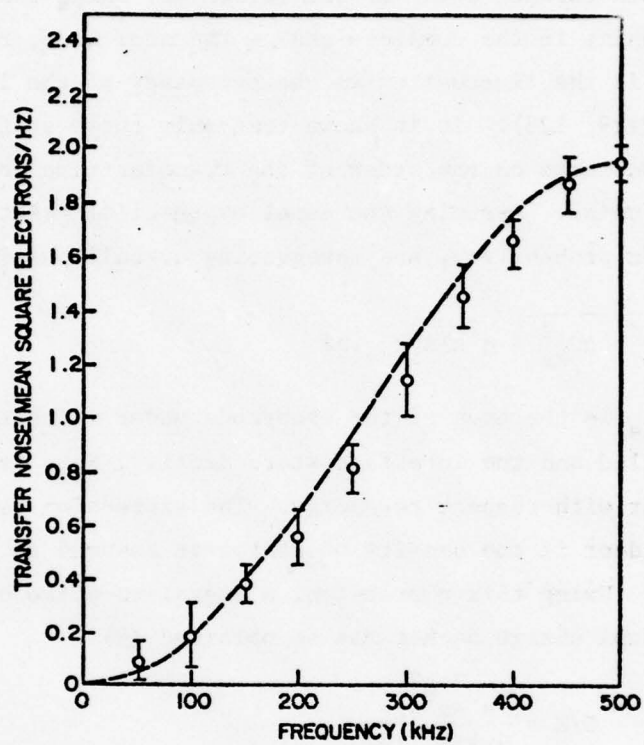


Figure 3.39. Spectral distribution of transfer noise measured on a 3-phase surface channel CCD at 1 MHz (after 126).

levels, the total transfer noise of a bulk channel is give by (122)

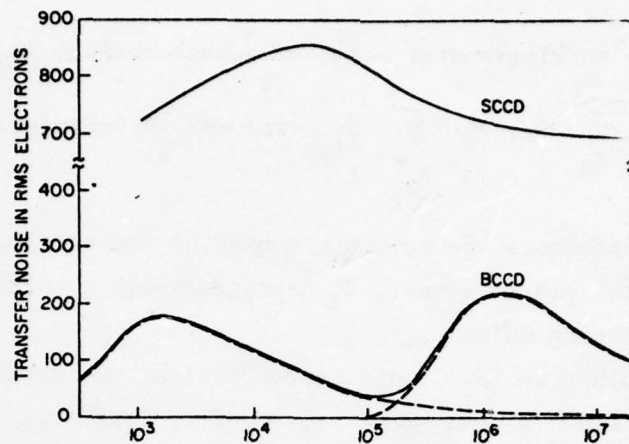
$$\overline{\Delta Q_{t_b}^2} = 2nq^2V'_S \sum_{\tau_{b_k}} N_{t_k} \exp(-t/\tau_{b_k}) [1 - \exp(-t/\tau_{b_k})] \quad (3.79)$$

where V'_S represents the volume occupied by the charge. It is seen that with decreasing signal, V'_S decreases with a corresponding decrease in bulk trapping noise.

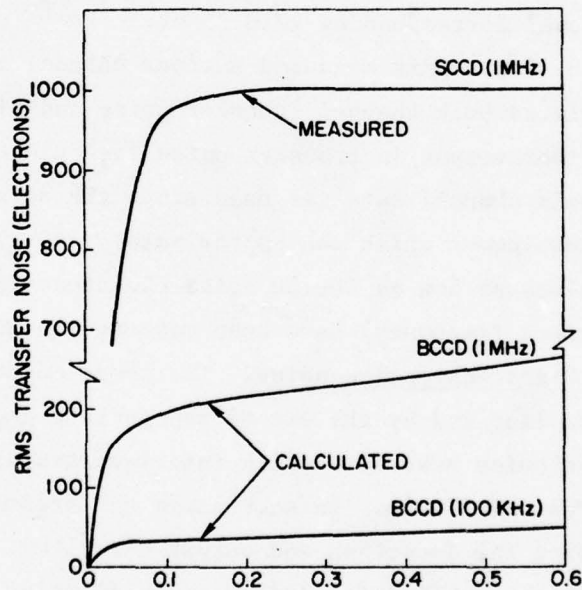
The bulk trap levels and concentrations are not well understood nor controlled. In many devices, however, levels at 0.25 and 0.54 eV below the conduction band are found to be major contributors to trapping noise. Concentrations of these traps were found to vary from batch to batch between $5 \times 10^{10} \text{ cm}^{-3}$ and $1 \times 10^{12} \text{ cm}^{-3}$ (128). Gold has been identified as a major source of noise (129). It is to be noted that Au has an energy level 0.54 eV below the conduction band in Si, but no level corresponding to 0.25 eV.

Figure 3.40 presents measured surface channel transfer noise data versus calculated bulk channel transfer noise and illustrates the theoretical improvement in transfer noise for bulk channel devices. Calculated bulk channel data was used since the data was below the limit of the test equipment which was approximately 200 electrons. More recently, values as low as 10-100 noise electrons (depending on signal charge and clock frequency) have been measured in BCCD's (128).

3.4.4. Signal detection noise. The above noise sources can be reduced by cooling and by the use of appropriate geometry and input methods. The noise associated with interface trapping can be eliminated by the use of BCCD's. In such cases the predominant noise is associated with the detection and output circuitry. Typical output methods use either a floating diffusion or floating gate to detect the presence of charge. In either case, the floating element must be periodically reset to some potential so that the next charge packet can be accurately sensed. The noise introduced by this resetting is



a) as function of clock frequency using measured surface channel data from 256 elements, 3-phase device versus calculated bulk channel data with two trap levels.



b) as function of size of charge packet using measured surface channel data versus calculated bulk channel data.

Figure 3.40. Total transfer noise for bulk versus surface channel CCD's (after 57).

the thermal noise of the MOS channel resistance in parallel with the floating diffusion capacitance; or the thermal noise of the resistance through which the floating gate is reset (125). In order to achieve low values of reset noise, on-chip preamplifiers are often used in conjunction with filters, and the reset MOSFET is operated in saturation since the triode mode provides excessive noise due to the partitioning of the channel charge between the floating output node and the reset voltage supply (57). A theoretical study of optimum detection methods has been made using various filtering and integration techniques originally developed for nuclear electronics (9).

Considering techniques which have been implemented, correlated double sampling (66, 130) removes the switching transients at the detection node and eliminates the reset noise. This method also suppresses surface state and $1/f$ noise contributions. However, the signal is derived from a subtraction of two measurements which leads to a loss of a factor of $\sqrt{2}$ in signal-to-noise ratio. A rms detection noise of 135 electrons has been reported using a 64-element linear image sensor operating at $f_c = 50$ kHz with output capacitance of 0.25 pf.

Floating gate amplifiers, as described in chapter 2, yield low noise values because of the small total capacitance of the detection node and because the reset noise can be avoided. The noise measured experimentally in a 12-stage distributed floating gate amplifier at 1 MHz was approximately 10 to 50 rms electrons which, because of the \sqrt{n} or $\sqrt{12}$ noise improvement, theoretically results in about 50 rms electrons per individual state (72, 75). It is thought that the sampling rate could be increased to about 7 MHz without altering the signal or noise level. It is speculated that, with a cooled distributed floating gate amplifier with enough stages, a single electron could be detected.

3.4.5. Comparison of noise sources. A comparison of the relative importance of the various noise sources has been made which also

illustrates the differences between SCCD's and BCCD's (127). Table 3.3 illustrates experimental results for 256-element CCD's clocked at 1 MHz with an active electrode area of $6000 \mu\text{m}^2$. It is seen that dark current noise is larger in BCCD's than in SCCD's (because of the larger depletion region width). In all other categories the noise in BCCD's is smaller or equivalent to that in SCCD's.

TABLE 3.3

Measured Noise Levels in 256-Element CCD
At 1 MHz Clock Frequency (in electrons)
(Active Element Area $200 \times 30 \mu\text{m}^2$)
 (after 127)

Noise Source	Noise Equivalent Signal in SCCD	Noise Equivalent Signal in BCCD
Electrical Insertion Noise of Background Charge (FAT ZERO)	750	Not Required
Electrical Insertion of the Signal Charge	750	750
Optical Injection of 1 pC of Signal Charge	2800	2800
Trapping Noise ($N_{ss} = 1 - 2 \times 10^9 \text{cm}^{-2} \text{eV}^{-1}$)	700-1000	<200
Dark Current Noise	160	320
On-Chip Amplifier Reset Noise $C_0 = 0.7 \text{ pF}$	~ 330	~ 330
Pulser Noise with Off-Chip Preamplifier	440	440
Pulser Noise with On-Chip Preamplifier	<30	
Maximum Signal in Electrons for $V_p = 14 \text{ V}$	40×10^4	20×10^4

3.5. Power Dissipation

One advantage of CCD's is their low power dissipation due to the absence of quiescent currents while the charge packets are stored in the potential wells. This fact becomes particularly significant in large area systems such as memories. Power is consumed by recirculation and refreshing circuits in memories. During the actual charge transfer, some power is dissipated in the bulk silicon to move the mobile carriers into potential wells, but most of the power is dissipated in switching the electrodes between clock potentials. This is mainly reactive power depending on the design of the drivers. In many CCD chips, more of the power is dissipated in the associated peripheral MOS circuitry than in the CCD section itself. First-order calculations have been made for the internally dissipated power and the external power (9, 131, 132).

When internal power dissipation occurs, the carriers are moving through a crystal lattice and are reacting with the lattice. Power is dissipated because of the motion of the charge packet and similarly due to the motion of the majority carriers which must move to change the depletion widths. If majority carriers come from adjacent electrode areas as the potential well is shifted through the array, then the majority carriers move in the opposite direction to the motion of the potential well. Since the depletion width decreases as signal minority carriers increase, the magnitude of majority carrier decreases with increasing signal charge.

The motion of the charge carriers has been idealized by assuming that a CCD could be approximated by a traveling-wave device of velocity v (131). Assuming that the carrier velocity is constant ($v = f\lambda$) where λ is the wavelength and f is the operating frequency, then the lower limit of the dissipated power required to move a signal, charge Q'_n is

$$P = Q_n' v^2 / \mu = Q_n' \lambda^2 f^2 / \mu \quad (3.80)$$

where μ is the mobility. If no signal charge is present, then only the majority carriers move and must fill $\Delta Q = \Delta X_d N_A$ locations where ΔX_d is the change in the depletion width. So similarly,

$$P = \Delta X_d N_A v^2 / \mu_B = \Delta X_d N_A \lambda^2 f^2 / \mu_B \quad (3.81)$$

where μ_B is the bulk mobility since the change in the depletion width occurs in the bulk. The mobility μ in Eq. 3.80 is the mobility of the free carriers in the channel, i.e. surface mobility μ_s for surface channel devices and μ_B for bulk channel devices.

Another way of representing the power dissipated as signal charge moves through the array is to calculate the energy dissipated in moving charge over a potential step $\Delta\phi_s$ into a deeper potential well. Considering an n phase device, an upper bound to the power dissipated is

$$P = n f C_n' Q_n' \Delta\phi_s \quad (3.82)$$

Since the potential considerations change for CCD's with different number of phases, equation 3.82 must be modified accordingly. For two-phase devices, as charge fills the potential well, the effective barrier height changes. For three-phase and properly clocked four-electrode two-phase devices, the situation is different since the initial charge starts to move before the total potential well has formed and thus moves through a smaller potential difference. These devices should more closely approximate the power dissipation of the traveling-wave case.

Finally, there is sizeable reactive power associated with the charging and discharging of the electrodes during each clock cycle. The actual amount of power dissipated depends on the design of the driver since most of the reactive power is dissipated in a resistive driver, while much less reactive power would be dissipated in a tuned LC driver. Assuming a resistive driver design and an electrode capacitance $C' (\sim C_{ox}'$ for high resistivity substrates), then the dissipated power in the clock circuits is given by

$$P = fc'v_p^2$$

(3.83)

Roughly, the internal dissipation for normal size devices range from low nW range to low μ W range per cell. Depending on the driver design, clock power is normally in the range of tens of μ W per cell.

4. CIRCUITS

4.1. Digital Circuits

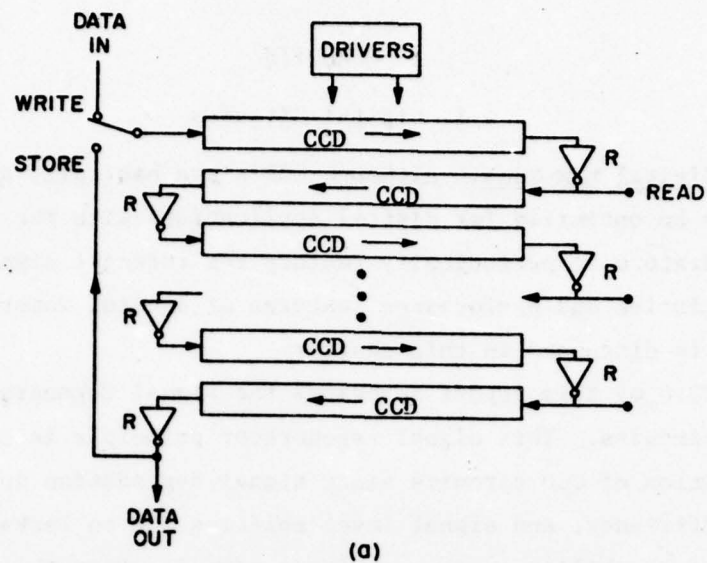
4.1.1. Digital Memories. Although CCD's are basically analog devices, they can also be optimized for digital applications with the addition of signal regenerators to periodically restore the internal signal levels. The characteristics and performance features of digital memories using this concept is discussed in this chapter.

Section 2.6 of this report describes the signal regenerator used in digital CCD circuits. This signal regenerator principle is the key to digital operation of CCD circuits since signal degradation due to charge transfer inefficiency, and signal level shifting due to leakage, both result in loss of ability to detect binary signals after the signal has passed through many stages of CCD circuitry (29,48,64,68,78-82,95,150,151). Many large digital CCD circuits will require signal regeneration, and regeneration techniques cannot be neglected in digital CCD development.

The CCD device is basically a serial transfer circuit and when used as a memory, it is almost always used as a serial memory. However, within the realm of serial memories there are many possible organizations of the device bit structure.

4.1.1.1 Memory organizations. a) Serpentine organizations. The serpentine serial memory organization (Fig. 4.1) was the concept which received the initial effort in digital CCD memory development since it naturally evolves from the basic serial analog delay line. In this organization the signal regenerators (R) regenerate the binary information after a number of transfers (48,78,80,95,151,152). In a memory organization of this type, the maximum storage on the CCD integrated circuit is no longer limited by analog considerations such as charge transfer efficiency and dark current but is limited only by the maximum chip size which can be processed with usable yield.

A current example of a serpentine organization (48) is a 4160 bit C4D serial memory. The organization of this chip is shown in Fig. 4.2. The chip consists of 4160 C4D cells divided into two 2080 bit halves.



(a)

Figure 4.1. Serpentine serial memory organization showing CCD delay lines and signal regenerators (R) (after 9).

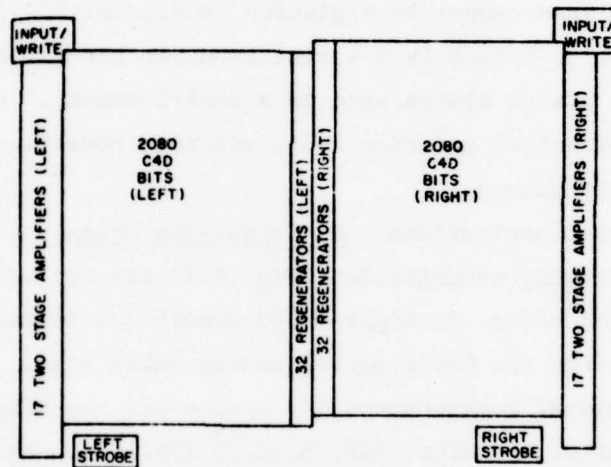


Figure 4.2. Chip organization of a 4160 bit C4D serpentine serial memory (after 48).

Since C4D technology requires only two phases, the opportunity was taken to alternate the ϕ_1 and ϕ_2 clocks on the two halves of the chip thereby doubling the effective frequency of operation using a multiplex-like technique. For instance, on one half of the chip the input and output occur on ϕ_1 whereas on the other half they occur on ϕ_2 . Thus two bits of data enter or leave the chip on each clock cycle. Since the multiplexing consists of only two paths, the multiplexing and demultiplexing circuits are extremely simple.

This serial memory has an output tap every 130 bits for a total of 32 outputs. Accordingly, at an input data rate of 3.2 MHz (clock frequency of 1.6 MHz) the maximum access time to any bit is 81 microseconds. Internally, the data is refreshed every 65 bits. At the end of each half of the chip the data is regenerated and delivered back to the input for continuous recirculation until new data is written into the memory from an external source. Even though the C4D transfer efficiency is only 99.8 to 99.9% per transfer, at data rates below 2 MHz, the refresh after every 65 bits results in adequate digital performance. Tests on the fabricated circuit indicated acceptable performance of data rates from 2 KHz to 3.2 MHz at 25°C. The power required to operate this circuit was 0.5 μ watt per bit at 100 KHz data rate to 16 μ watts per bit at the 3.2 MHz data rate. The chip layout occupies an area of 4.6 mil² per bit. A basic disadvantage of this design is the necessity of external addressing of each of the 32 output taps in order to achieve the 80 microsecond bit access time. An additional disadvantage of this design is that the output taps do not decrease the write access time. The maximum access time to address a particular bit for writing new data is 1300 microseconds, which is prohibitive in many applications.

b) Loop organizations. A typical loop serial memory organization is shown in Fig. 4.3. This organization is also known as Block Addressing or Line Addressing and includes many of the features of the serpentine organization with the added feature that the logic required to address a particular line or track of CCD storage elements is integrated on the CCD storage chip. This greatly reduces the quantity

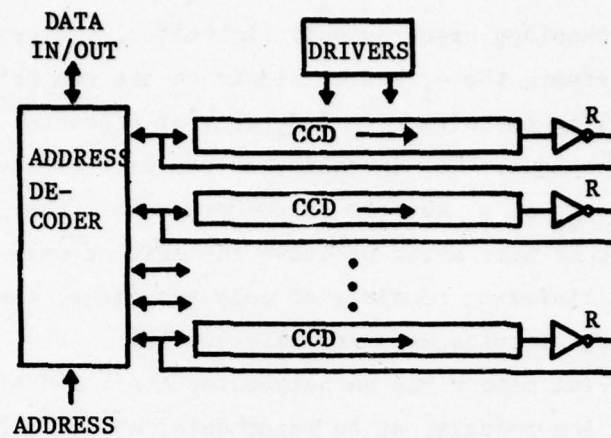


Figure 4.3. CCD memory loop organization (after 44).

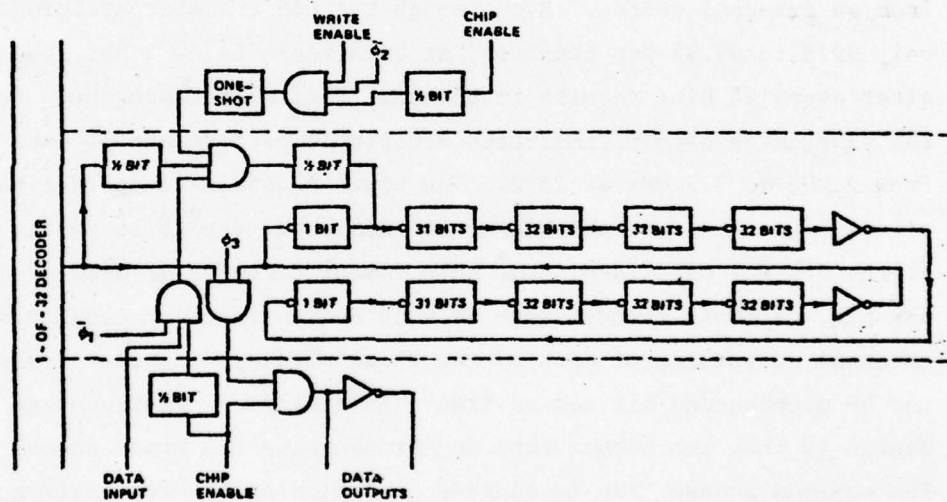


Figure 4.4. One 256 bit track of a loop organized serial memory (after 153).

of external circuits required to address the memory. This organization also reduces the write access time since the read and write circuits on the chip are both addressed by the same decoder.

A current example of a loop organization is an 8192 bit serial memory (153). This memory is divided into 32 tracks of 256 bits each, with access to any track through an on-chip decoder for reading or writing. The organization of each track of this device is illustrated in Fig. 4.4. Each track is a recirculating loop consisting of two rows of 128 bits each. Each row is further broken down into sections of 31 or 32 bits, each with regeneration between each of these sections. The relatively small number of stages between regenerations was selected to provide good low clock frequency performance. This chip was designed and processed with a 2 phase 2 level polysilicon gate n-channel CCD process. The power required for this circuit is 30 μ watts per bit at 1 MHz clock frequency and 0.6 μ watts per bit at 20 KHz clock frequency. The chip layout occupies an area of 3.6 mils²/bit.

Another current example of a loop or line addressed serial memory (154) is presented in Fig. 4.5. This memory has four sections of 32 lines each, with each line consisting of 128 bits. Each section of 4096 bits has its own decoder, recirculation loop, data input-output circuits and charge regeneration circuit from 32. Figure 4.5 illustrates only one of the 4096 bit sections. The other 3 sections are identical. This circuit is processed with an isoplanar, n-channel, silicon-gate, buried channel, implanted barrier, and is unique in that only one clock is required for operation. The phase is operated by a DC voltage. The circuit is designed so that the clocks may be stopped for a period of time determined by the minimum minority carrier storage time in the circuit. This clock stopping provision allows synchronization of the circuit to a data rate other than the basic clock frequency and also to reduce power dissipation. In tests of this circuit, the clock has been stopped for periods in excess of 100 μ sec. at room temperature while still retaining data. The maximum access time to any bit in this design at a 5 MHz bit rate is 25.6 μ sec. The chip size is

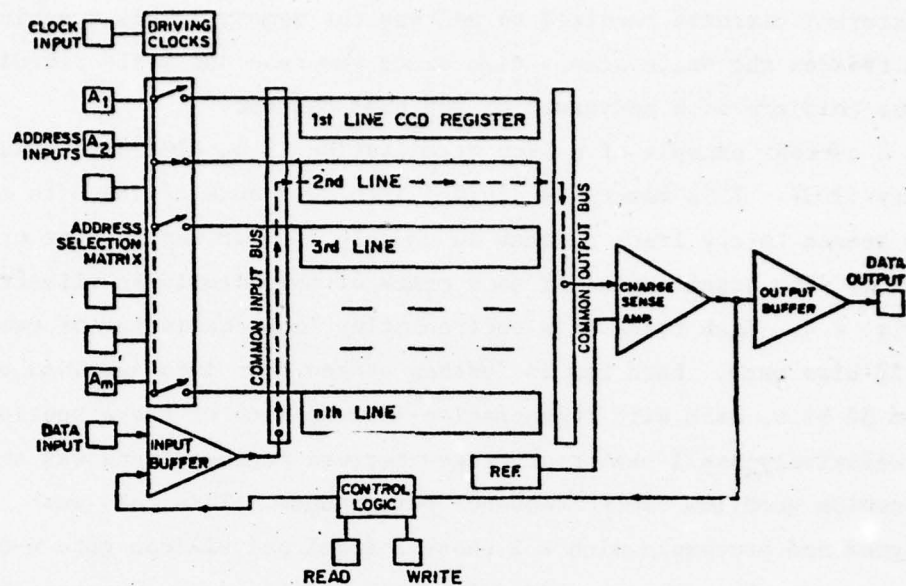


Figure 4.5. Basic organization of a 16,384 bit loop organized serial memory (after 154).

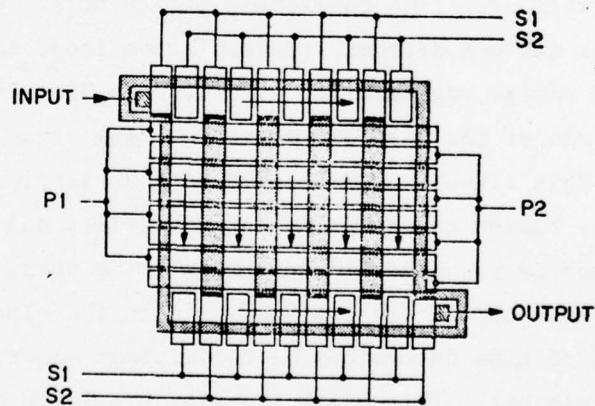


Figure 4.6. A typical serial-parallel-serial memory organization.

2.7 mil² per bit. The primary reason for this small chip size is the reduced number of regeneration circuits. In this approach only one regeneration circuit is used for every 4096 bits while most other reported designs utilize one regenerator for every 32 to 500 bits.

One major disadvantage of this design is the necessity for periodically cycling through all 32 line addresses to refresh the memory. This refresh is required for conventional MOS dynamic random-access memories. The refresh requires additional external logic and reduces the amount of time that the memory is available for memory access operations.

c) Serial-parallel-serial organization. A schematic of a typical serial-parallel-serial (SPS) memory (9) is shown in Fig. 4.6. In this memory the data is transferred into and out of the memory at the full data rate by the input and output serial registers at the top and bottom of the figure, which serve as data multiplexer and de-multiplexer, respectively. However, the majority of the storage occurs in the vertical serial registers which transfer data at a slower rate. For example, in a 64 by 64 array, if the input data rate is 1 MHz the vertical registers will be operating at a rate of only 1/64 of 1 MHz or approximately 16 KHz. Therefore, according to the power dissipation equation previously presented, the basic power requirement for such a register would be about 1/64 the power required for a simple serial register operating at a data rate of 1 MHz. This power reduction is one of the key features of the SPS organization.

Another feature is the reduction of the number of transfers required to pass a bit of data through the memory since each bit of data does not transfer through the entire memory as it does in a simple serial register. In the 64 by 64 SPS array example above, the total number of transfers of any bit from the register input to the register output would be $n(2 \times 64) = 128n$, where n is the number of phases used per stored charge packet. Since data degradation resulting from transfer inefficiency is greatly reduced due to the significant decrease in

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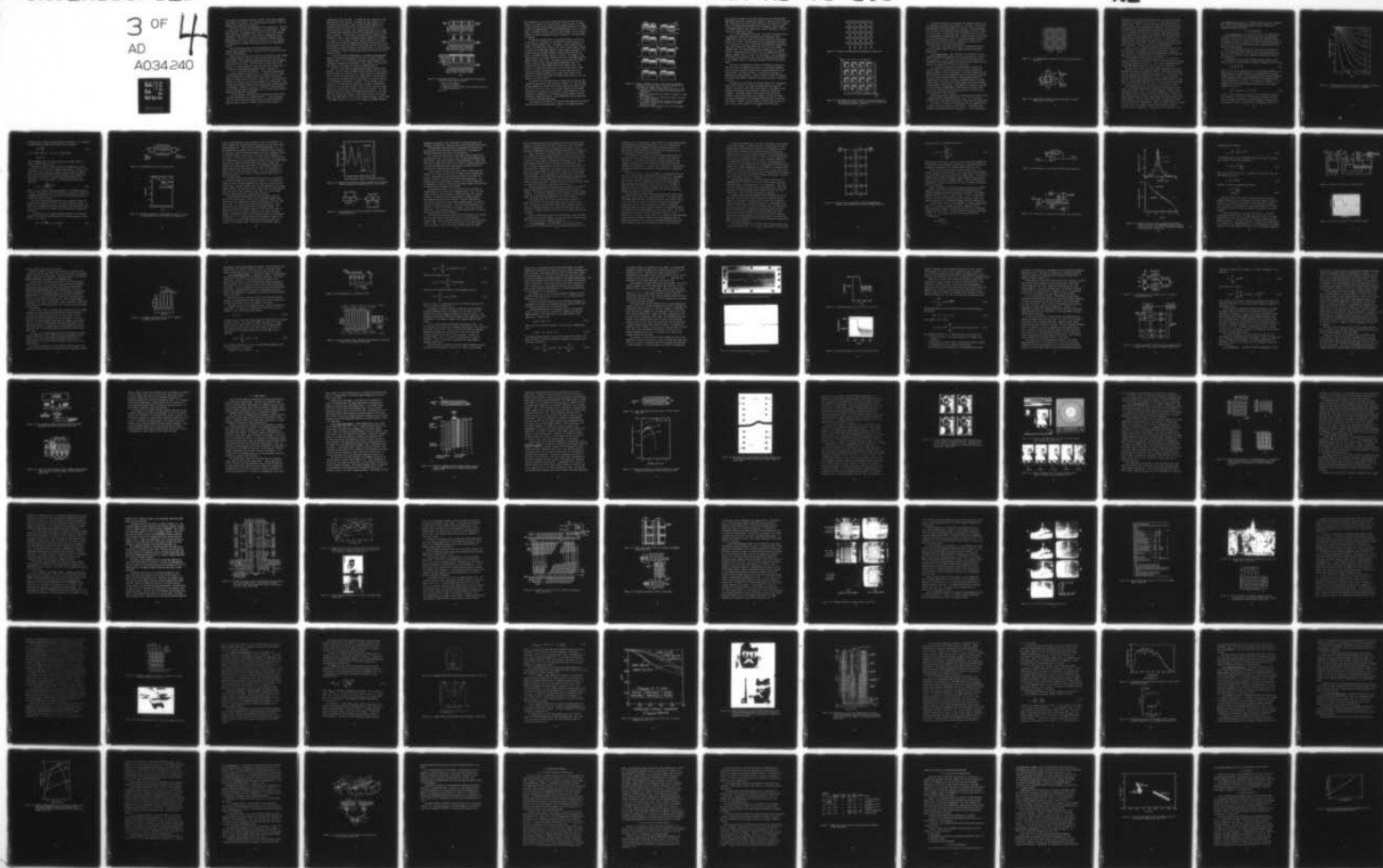
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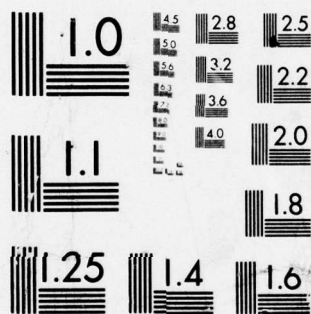
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total number of transfers from input to output, fewer charge regeneration circuits are required. The resulting chip is therefore smaller as compared with a simple serial register.

There are three major disadvantages of this organization. First is the long access time, which is identical to the access time of a simple serial register. The maximum access time for a 64 by 64 SPS register operating at 1 MHz would be 4.1 msec, which is prohibitive in many applications. This access time can be reduced by combining the SPS organization with the loop organization resulting in a chip organized as a multiplicity of smaller SPS registers which can be individually accessed.

The second disadvantage of the SPS organization is the more complex clock requirement (155). (Clocks are now required for both the fast and slow registers).

Third is the fact that since each bit of data does not flow through each storage element, variation in dark current across the chip, or local defects, can contribute different dark currents from one parallel vertical path to the other. This increases the noise level of the detector, or charge regenerator input, and increases the difficulty of the detector in distinguishing between a logic 1 and logic 0.

4.1.1.2. Nonvolatile CCD memories. In some memory applications, a nonvolatile memory is required, that is, a memory that will retain its stored data when the power supplies and clocks are turned off, either to conserve power or because of power outage. All semiconductor memories are volatile unless they are designed to be nonvolatile. Nonvolatile semiconductor memories always require special design techniques or technology. Examples of these are the fusible link and avalanche induced migration bipolar technologies, and the floating gate avalanche injection and MNOS MOS technologies.

In CCD technology, the nonvolatile technique which has received the most investigation is the MNOS structure. In this technology a very thin layer of silicon dioxide, usually less than 5nm thick is grown on silicon while 50 to 100nm of silicon nitride (Si_3N_4) is

deposited over the SiO_2 layer. A conventional gate conductor is then deposited over this structure. By biasing the gate conductor at a relatively high potential, charge from the silicon substrate or an inversion layer can be moved to the interface between the silicon dioxide and silicon nitride. This trapped charge results in a change in the MOS device threshold which can be distinguished from the normal device threshold. In this manner, the normal device threshold can be defined as a logic 0, and the modified device threshold can be defined as a logic 1, or vice versa, so that a digital memory bit is created. The device can be erased by applying the opposite polarity bias to the gate conductor so that the interface charge moves back into the silicon and the device threshold returns to its original value. By this technique it is possible to create a digital memory which will retain its stored states for years.

In the CCD nonvolatile NMOS memory, as in many conventional MNOS memories, an additional mechanism is also used to control the MNOS charge storage. Since the CCD device utilizes charge packets to store information, reading the charge packet in the silicon is used to determine whether or not charge is stored in the MNOS interface.

There are several ways of implementing the MNOS structure in CCD memories. One is to place the MNOS structure directly over the charge transfer channel of the device (156). This technique is represented in Fig. 4.7a where the dotted areas are the MNOS gates. The bit pattern to be stored in the MNOS devices is transferred to the proper position in the CCD memory using normal techniques. The bit pattern is then written into the MNOS device by raising the voltage of the MNOS gate electrodes to a high value (20-30V). Where the cell contains a charge packet, the voltage drop is primarily across the insulator. The high insulator field pulls charge to the MNOS interface where it is stored. Where the cell does not contain a charge packet, much of the voltage drop in the MNOS device is in the silicon depletion region, and the field in the MNOS insulator is too low to pull charge to the MNOS interface.

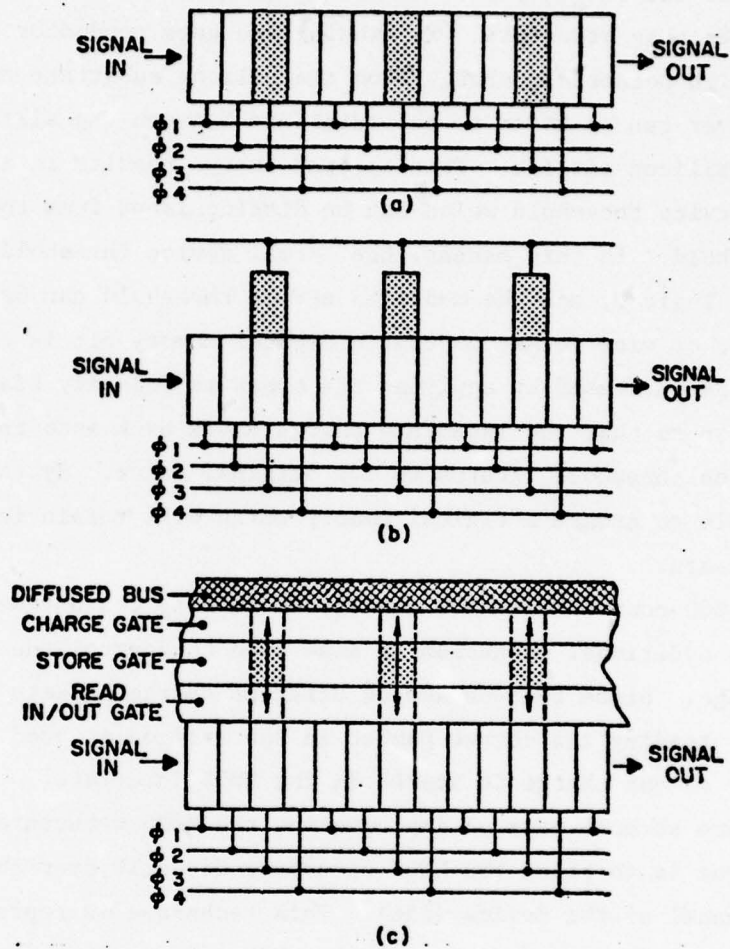


Figure 4.7. Use of MNOS technology to form nonvolatile CCD memories. The MNOS storage cells are placed:

- a) In the CCD channels
 - b) Next to the channel
 - c) Separated from the channel and the input bus line by extra transfer gates
- (after 9)

The information is read out by filling the entire CCD structure with charge. The voltage on the CCD electrodes is then reduced, and charge is driven into the silicon substrate at the MNOS sites which have charge stored in the MNOS insulator. Those MNOS sites which do not have charge stored in the MNOS insulator retain the filled charge. The CCD charge packets can then be transferred through the memory in the normal manner for reading.

An improved technique (157) is illustrated in Fig. 4.7b and 4.8. In this case, the information is transferred in the CCD memory by the normal procedure (Figure 4.8a). The charge is then transferred laterally to the MNOS devices (Figure 4.8b), while a high voltage (20-30V) is applied to the MNOS gate conductor. Where charge is present in the silicon substrate, the MNOS insulator field is high, and charge is moved to the MNOS insulator, where it is stored. The absence of CCD charge results in a low MNOS insulator field and in zero MNOS insulator charge storage (Figure 4.8c). The memory is then filled with charge. However, charge is only retained under the MNOS gates where the insulator does not contain MNOS stored charge (Figure 4.8d). For readout, the conditional charge stored in the silicon under the MNOS device is laterally transferred back to the CCD device where it is transferred through the memory in the normal manner (Figure 4.8e). Note that in both of these cases, the readout logic states are the complement of the input states.

The speed of the read and write can be improved by using the more complicated organization (158) presented in Figure 4.7c. Here the MNOS storage elements are isolated from the CCD channels with gates so that data can be read into or out of the transfer register while the MNOS storage sites are being written or erased. Excess charge from a write operation is transferred to the diffused bus, and charge for reading can also be taken from this bus. This organization is less dense than the previously described approaches.

Test structures of from 3 to 64 bits have been fabricated and tested using all three of these approaches. However, no commercial devices

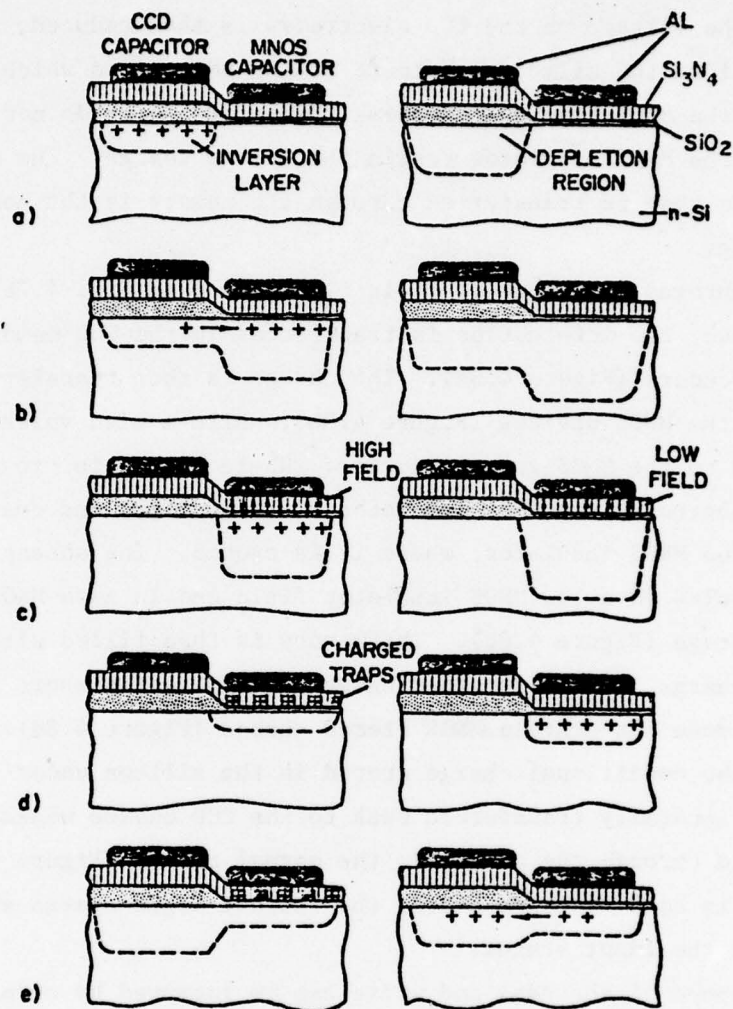


Figure 4.8. Combined CCD/MNOS structure illustrating the Read/Write technique for the logic ONE. Case (left column) and the logic ZERO case (right column). (after 157).

- a) Presence or absence of inversion layer under the CCD electrode (this is the state to be written into the memory bit).
- b) Transfer of inversion layer charge, if present, to the MNOS capacitor.
- c) Gate stress results in conditional transfer of charge to the MNOS interface.
- d) For readout, charge is only retained under the MNOS electrode if charge was not tunneled to the MNOS interface in step c.
- e) Conditional charge transfer back to CCD for readout.

are available, probably for the same reasons that few conventional MOS MNOS memory devices are commercially available. Nitride storage structures with reproducible electrical characteristics are very difficult to manufacture, and degradation mechanisms such as permanent charge trapping in the MNOS insulator exist, which must be better understood before the devices are commercially viable.

4.1.1.3. Two-dimensional CCD arrays. Since most CCD devices have a one-dimensional signal flow resulting from an essentially linear organization of the array, most of the devices described in this paper utilize this concept. The serpentine and loop organizations described in this section all utilize an essentially one-dimensional organization where each storage cell communicates with only one of its adjacent neighbor cells. The serial-parallel-serial organization is a special case of a two-dimensional array where a cell can communicate with two adjacent neighbor cells in a very structured manner. The two dimensional concept can be expanded so that a cell can communicate with several of its neighbor cells in a fairly general manner (159) as illustrated below.

The general two-dimensional concept is illustrated in Figure 4.9 where each cell can communicate with each of its adjacent neighbors, even those which require a reverse flow of charge as indicated by the double arrows. The shift direction is controlled by selecting the appropriate clocking sequence. Using the original 3-phase CCD concept, this array would require 5 separate clock phases and would be difficult to lay out.

An extension of the 2-phase CCD concept suggests the 2-dimensional array shown in Figure 4.10, where the hatched areas are potential barriers that give the cells their directionality. The number in each storage cell indicates the clock phase to which the electrode is connected. The minimum number of clock phases that provide full freedom of selecting the direction of transfer is three, but charge can only be transferred in two orthogonal directions due to the potential barrier. However, the array layout is denser than the array in Fig. 4.9 due to the reduction in the number of clock bus lines.

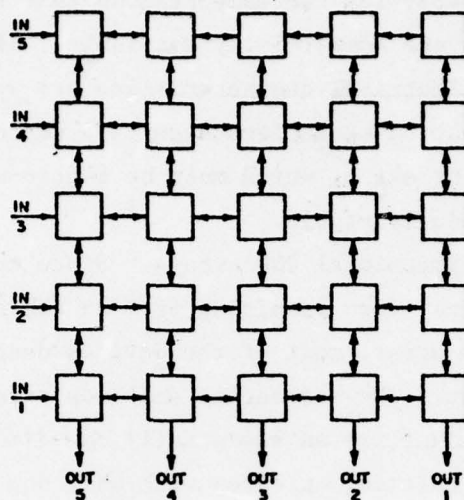


Figure 4.9. General two-dimensional CCD organization (after 159).

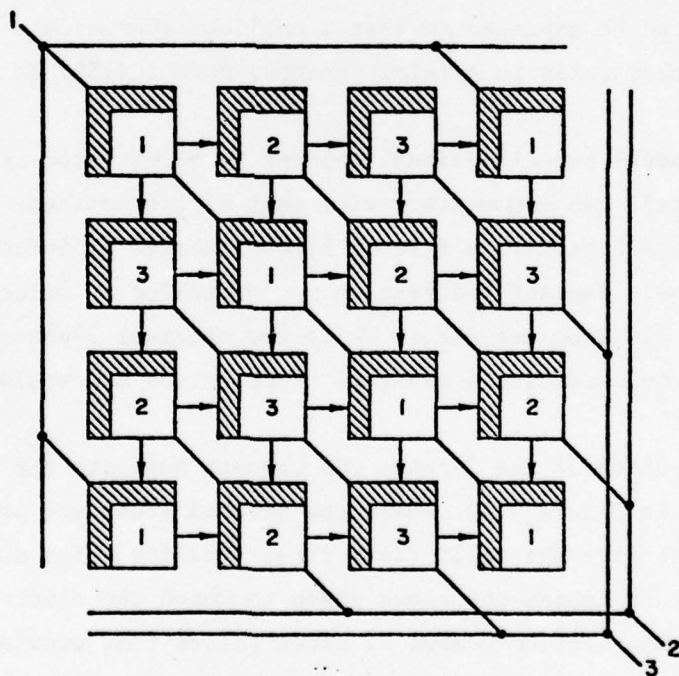


Figure 4.10. Two-dimensional charge transfer array with three sets of directional electrodes. This array can shift signals in two orthogonal directions (after 9).

The arrays described are the densest organizations possible since all electrodes are identical and because it is possible to perform the two-dimensional switching operation in each cell. Many applications may not require this flexibility and an arrangement as shown in Figure 4.11 can be used. In this array, only the special cells "S" perform the two-dimensional switching function. Ordinary linear transfer cells are located between the "S" cells. A mass serial-parallel converter might use this organization where the direction of signal flow is again determined by the clock phase sequence.

There are of course many other forms of two-dimensional arrays which are possible (159) for use in signal processing and imaging applications.

4.1.2. Logic Arrays. Logic functions in CCD arrays can be performed by providing the capability for CCD charge packets to interact with one another. If these logic functions can be performed while retaining the processing simplicity and layout density inherent in CCD devices, the concept will be useful in CCD arrays.

It is obvious that logic can be performed in CCD arrays with circuits similar to those which are used for charge regeneration, address decoding, and output buffering. One concept proposed (82) was the connection of the two regeneration gates to the sensing diffusion of the two charge transfer channels. These regenerators would be connected either in series or parallel determining whether a charge packet would be injected into the output channel, and thus performing a logical NAND or NOR function. This approach is essentially the same as the well-known standard NAND and NOR functions performed by MOS logic using conventional MOS technology and does not fully utilize the high density of CCD technology.

Direct charge packet interaction can also be used to perform logic. A proposed method of accomplishing this is the use of a metering potential well to determine the presence of more than one charge packet.

The layout of a 2-phase CCD logic gate which can perform AND and OR logic is shown in Figure 4.12 (117,160,161). The dashed lines represent conventional CCD potential barriers. In this illustration,

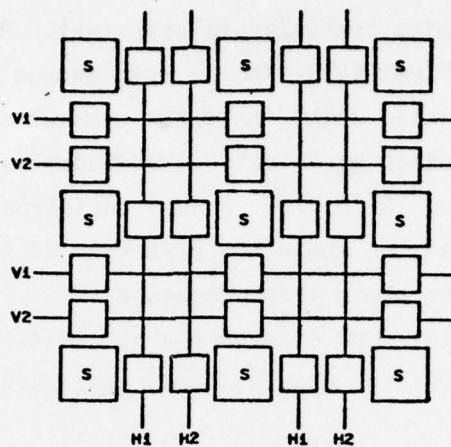


Figure 4.11. A two-dimensional organization with only one switch point per cell.

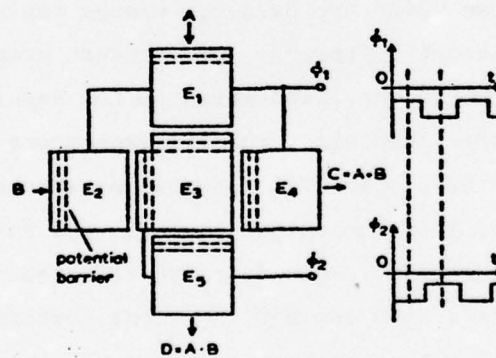


Figure 4.12. Organization of charge transfer electrodes to perform binary logic (after 161).

electrodes E1, E2, and E4 are connected to the ϕ_1 clock and electrodes E3 and E5 are connected to the ϕ_2 clock. The clock pulses assume p-channel devices. When ϕ_1 is high, the charge under electrodes E1 and E2 is transferred to the potential well under E3. The barrier between E3 and E4 prevents charge transfer between the E3 and E4 electrodes. If it is assumed that both E1 and E2 contain a logic ONE (are filled with charge), then the potential well under E3 fills up and the extra charge spills into the potential well under E5. If either E1 or E2 contains a ONE, the potential well under E3 fills up, but there is no extra charge to spill into E5. Thus, E5 contains a ONE only when both inputs are ONE's. The array thus performs an AND function.

When ϕ_1 is low, no charge transfer occurs between E3 and E1, and E2 or E5, due to the presence of the potential barriers. However, the charge due to a logic ONE under E3 is transferred to E4 and drained away, and the gate is primed for the next operation.

This logic gate also performs an OR function. The OR function output is obtained from electrode E4, which, as described above, receives any charge contained in E3 when ϕ_1 is low. E4 will therefore receive a logic ONE whenever either E1 or E2, or both, are a logic ONE.

Multiple cells of this type, when properly connected, can produce multiple-input AND, OR or combined functions. With slight modification, they can also perform threshold logic functions (9). When cells of this type are combined with regenerator or inverter circuits, arithmetic operators such as adders and multipliers can be obtained (162). An estimate of a 4x4 multiplier indicated that it would occupy about 1000 mil² of chip area and require 290 μ W of power at a clock rate of 1 MHz.

The combinational logic functions which have been described here utilize the inherent high density of CCD technology. However, several disadvantages exist. First, the incoming information is destroyed so that signals cannot be fanned out to several logic inputs. Second, and along the same line as the first disadvantage, they lack gain which also limits fannout. To drive several logic inputs, a charge packet would require subdivision or regeneration. Third, the proper transfer of charge in a logic array with complex interconnections would be extremely difficult without regeneration. Fourth, there is no known way to form

the complementary operation, i.e. inversion without the use of regenerators. All of these disadvantages limit the density which can be obtained with CCD logic arrays.

4.2. Analog Circuits

4.2.1. Analog Delay. The three basic functions of analog signal processing with CCD devices are analog time delay, multiplexing and filtering. Filters can be further subdivided into recursive filters and transversal filters. However, all of these analog applications rely on the fact that CCD devices provide accurate, clock-controlled time delays of analog signals.

Most of the information needed for the design and evaluation of CCD's for analog delay applications has been previously presented in this report and therefore, only a summary of analog delay using CCD's will be made here.

The maximum theoretical delay bandwidth product, $T_d B$, of a CCD delay line with one signal channel containing N elements or unit cells is

$$T_d B = \frac{N}{f_c} \frac{f_c}{2} = \frac{N}{2} \quad (4.1)$$

where f_c is the clock frequency and $f_c/2$ is the Nyquist frequency - the maximum theoretical signal bandwidth. The maximum number of stages through which the signal can be transferred without incurring additional loss in bandwidth due to transfer inefficiency is determined by the transfer inefficiency per stage, ϵ , and the number of phases, p . An expression for the inherent frequency response of a circuit with n elements is (95,164)

$$R(f) = \exp[-Np\epsilon(1 - \cos 2\pi f/f_c)] \quad (4.2)$$

A plot of this equation is seen in Fig. 4.13 for different values of $Np\epsilon$. Equation 4.2 and Figure 4.13 correspond to Equation 3.14 and Figure 3.9 respectively with the number of stages n replaced by Np . An evaluation of Eq. 4.2 indicates that the amplitude response of a

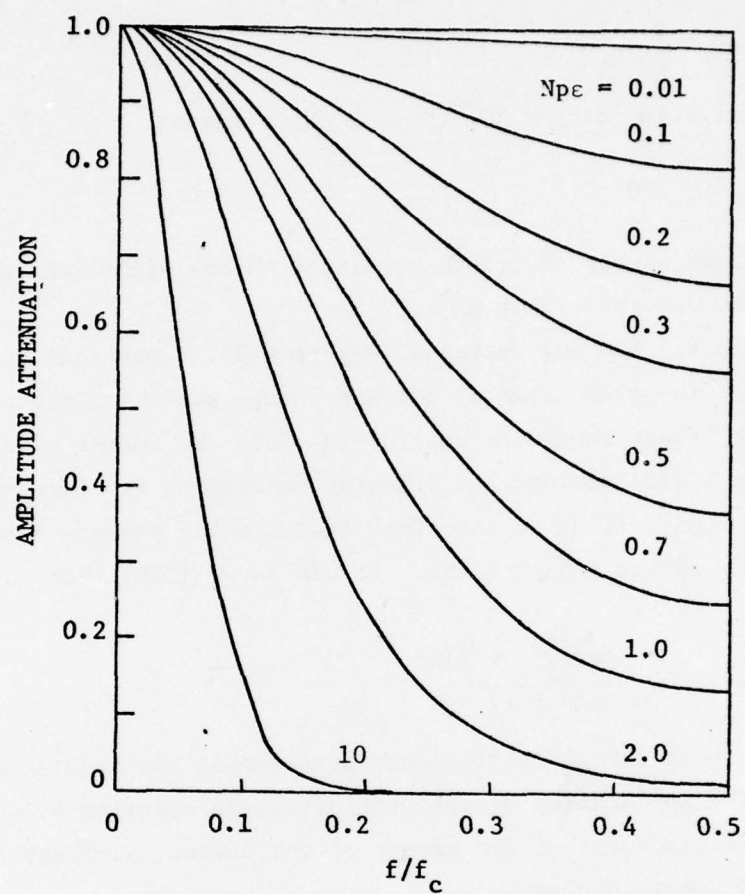


Figure 4,13. Amplitude attenuation as function of frequency with transfer inefficiency of a stage $Np\epsilon$ as a parameter.

CCD delay line is reduced by approximately 3db when $Np\epsilon = 0.2$. Therefore, by substitution, the upper limit for $T_d B$ can be defined as

$$T_d B = \frac{0.2}{2p\epsilon} \quad (4.3)$$

For a typical value of $\epsilon = 10^{-4}$ in a 2 phase device,

$$T_d B = 500$$

and the maximum number of stages permitted in one signal channel is $2(T_d B) = 1000$ for this value of ϵ .

Equation 4.2 and the curves of Figure 4.13 assume that ϵ is not a function of the time interval between charge packets. Actually, this second order effect should be considered since the amount of charge that is left behind during each transfer depends on the intervals of time between the filling of interface states which depend on the frequency, f , of the input signal. It was shown (119) that in the worst case

$$\epsilon(f) = \epsilon_n \frac{\ln\left(\frac{pfc}{2f} + 1\right)}{\ln(p + 1)} \quad (4.4)$$

where ϵ_n is the transfer inefficiency measured at the Nyquist frequency $f = f_c/2$. The application of this correction to equation 4.2 would cause a downward displacement of the center of the curves, although the end points would remain unaltered.

The delay limitations described above can be reduced by using the multiplexed CCD configuration (Fig. 4.14) with M parallel channels. In theory this configuration allows the $T_d B$ product to be increased M times since the total number of transfers of any charge packet is reduced by the factor M .

An expression for the inherent frequency response of an N element analog CCD incorporating multiplexing with M parallel channels as shown in Fig. 4.14 is (165)

$$R(f) = \exp\left[-\frac{Np\epsilon}{M}(1 - \cos 2\pi Mf/f_c)\right] \quad (4.5)$$

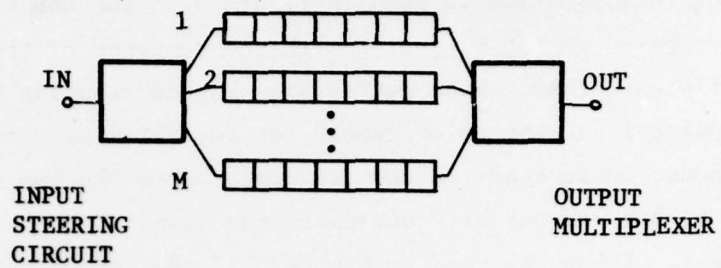


Figure 4.14. Multiplexed CCD delay line (after 165).

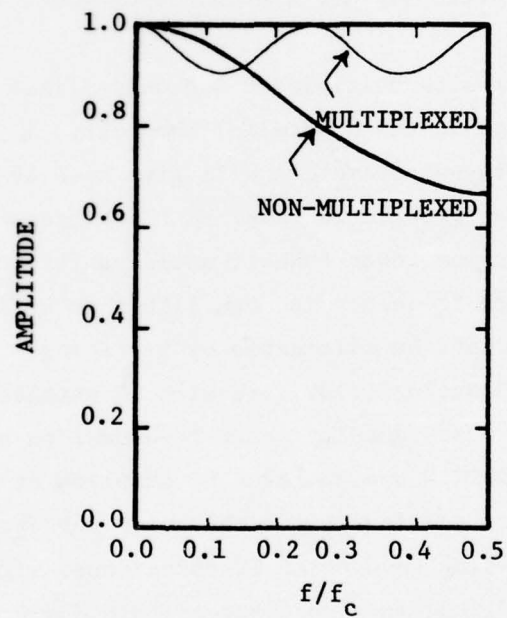


Figure 4.15. Frequency response of a multiplexed CCD with $M = 4$ and a non-multiplexed CCD, both for $N_{pc} = 0.2$ (after 164).

A plot of this equation is seen in Figure 4.15 for the case with $M = 4$, and is compared on the same plot with the response of the single channel, non-multiplexed case. Both curves are plotted assuming $N_{pe} = 0.2$. In most applications, the major reason for not allowing the high frequency CCD response to decrease beyond 3db compared to the low frequency response is that high frequency attenuation of the signal causes dispersion of the signal. It can be seen in Figure 4.15 that since the multiplexed CCD has a significantly better high frequency response than the non-multiplexed CCD, much less signal dispersion would result from the former case. However, when viewed in the time domain, the dispersion or smearing of signal charge in the multiplexed case will show a trailing signal M sample intervals after the primary signal. Thus, if a multiplexed CCD were used to delay a video signal, a bright spot would give rise to a ghost M samples away.

The major problem with multiplexed CCD delay lines is the matching of the gain and leakage in the M parallel channels. A very slight imbalance in either of these parameters will give rise to periodic fixed pattern noise. Another problem is that the clock frequency of the signal channels will be $1/M$ times lower than it would be for the non-multiplexed case. This lower clock frequency is then likely to be in the signal frequency range and cannot be eliminated by filtering.

A multiplexed CCD analog delay line with 10 parallel channels, each 64 bits long was used to delay color TV bandwidth signals (166). Adequate color TV bandwidth was achieved by sampling at either 10.7 MHz or 14.3 MHz, i.e. three and four times the color subcarrier. Phase behavior was good, passing good color TV chrominance signals. The measured and predicted frequency response of this device are shown in Figure 4.16 for the case where 8 channels of this device are multiplexed. The periodic valleys in the frequency response are as predicted by equation 4.5. The falling response with frequency is caused by the finite width of the input sampling window which was not taken into account in the predicted curve. The effect of differential channel

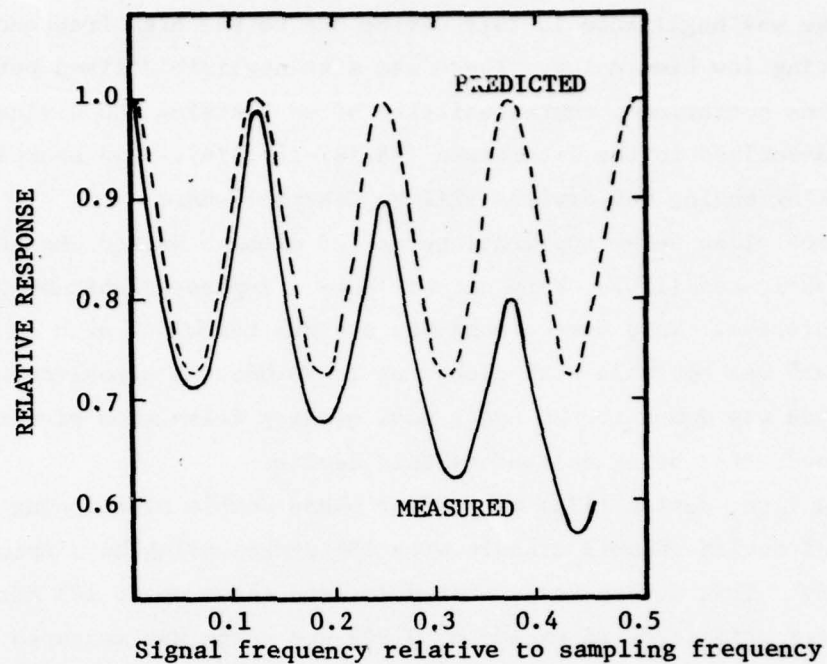


Figure 4.16. Predicted and measured frequency response of an 8 parallel channel multiplexed CCD analog delay line (after 166).

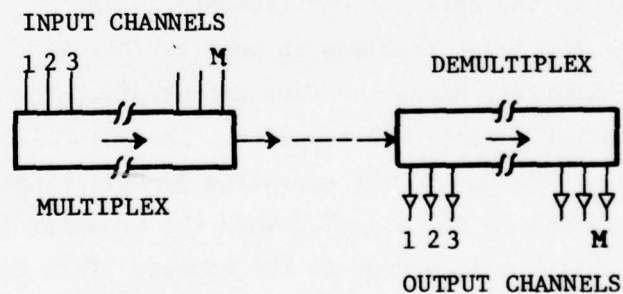


Figure 4.17. An illustration of the basic multiplex and demultiplex operation (after 9).

leakage was negligible in this device due to the high frequency and resulting low time delay. There was also negligible fixed pattern noise.

The performance characteristics of many analog CCD devices have been described in the literature (86,167-169,176). Two examples of operating analog CCD devices will be described here.

For video delay applications, a 128 element buried channel device was fabricated (170). This circuit used a 2-phase aluminum-polysilicon gate process. This device achieved a 4 MHz bandwidth at a 10 MHz clock rate and was operable with clocks up to 20 MHz. A signal-to-noise ratio of 42 dB was demonstrated and a good quality television picture was obtained after being delayed by this device.

A later device (178) was a four phase double overlapping gate N-channel buried channel circuit with 130 stages using an aluminum gate process. This device was operated at data rates up to 105 MHz and transfer efficiency in excess of 0.999 per stage was measured. It is believed that this device might be operable to at least 200 MHz with an improvement in the test circuitry since charge transfer efficiency did not degrade as the frequency was increased.

The maximum delay which a CCD analog delay line can provide is limited mainly by the dark current (leakage current) (179). The dark current causes the least problems in applications where the transfer frequency is constant, since the same amount of charge is added to each charge packet during each transfer. The major limitations in this case are a decrease in the operating dynamic range of the device and the noise added to the signal. When the transfer frequency is not constant, a "chirp" will appear in the signal. This is the case for delay time - axis conversion (2) or in signal buffers where the read-in and read-out frequencies are different.

One significant potential application for CCD delay is as a replacement for the ultrasonic delay line now used in the PAL System TV receiver (180). The chroma signal requires a 64 μ sec delay with a bandwidth of 1 MHz. If the 4.4 MHz local oscillator in the PAL system is used to generate 2.2 MHz clocks, then 141 delay stages are needed.

Since the ultrasonic delay line is selling for about \$1.00, CCD cannot compete at this price and if CCD are to replace it, they will probably have to be integrated with other functions in the receiver such as synchronous demodulation and color difference matrixing to be competitive.

Another application for CCD delay lines is scan conversion (180). As an example, in infrared imaging systems, the infrared detectors scan the scene with a horizontal sweep, and the output of each detector is clocked into a CCD capable of storing an entire display line. When the entire display frame is stored in the bank of CCD delay lines, the CCD's are read out sequentially and the video has the proper format to be displayed on a standard CRT. Two banks of CCD delay lines are used - while one is being loaded, the other supplies video to the CRT display. CCD's are limited in these applications to storage times of less than 100 milliseconds. This excludes some applications which require storage times of seconds, but the standard 525 line TV system frame time of 33 msec is within this limit. Storage times can be extended beyond 100 msec by cooling the CCD device to decrease the dark current.

Time axis equalization in both audio and video playback is another important application because a clock controlled variable delay is required. The time axis compression of speech signals, without frequency distortion to increase the playback word rate without the "Donald Duck" effect is another time axis application in this same category.

Gated analog delay can be used in moving target indicators in radar applications. In this application, the return signal from one pulse is subtracted from the return signal from a subsequent pulse. In this way, stationary targets are not seen and only moving targets are indicated. A similar technique can also be used to remove "ghosts" from TV signals.

Arrays of analog delay lines can be used in radar, sonar and scanning applications for beam forming, electronic focusing and beam steering. This is also of interest in medical applications.

4.2.2. Multiplexing. The multiplexing to be discussed in this section should be differentiated from the multiplexing discussed in the

previous section on analog delay. That referred to in the previous section was concerned with internal multiplexing to improve the operation of the CCD device without changing its signal processing function. In this section, multiplexing will be discussed as an operation used to obtain particular signal processing functions.

Multiplexing is an important signal processing operation and CCD multiplexers are and will remain prominent members of the family of CCD devices. As described previously the multiplex operation is performed by loading the CCD from a number of parallel inputs and then shifting the information out in serial form. Conversely, a demultiplexer is usually required in the system and it operates like the multiplexer in reverse.

If several channels of analog information are multiplexed into one CCD device, this is termed time division multiplexing (9). The sampled data in a time division multiplexed system is handled under digital logic control. The basic organization of CCD's to perform the multiplex and demultiplex operation is shown in Fig. 4.17. One sample is taken from each of the channels 1 through M, which are to be multiplexed. The samples are loaded in parallel into the CCD as shown and subsequently read out in serial form.

CCD multiplexing and demultiplexing devices have two unique limitations which must be taken into consideration (180). The first is that the charge inefficiency and resulting dispersion is more serious than it is in a CCD delay line since it introduces crosstalk between adjacent input/output channels. This problem may be solved by introducing isolation elements in between storage elements or by separating information samples by blank charge samples (9) in the CCD circuit. The second limitation is the introduction of fixed pattern noise due to non-uniformities in the gain or offset levels of the input and output amplifiers. However, improved CCD input techniques have been developed which are essentially independent of variations in the MOS threshold voltage and these techniques reduce the fixed pattern noise to a very low level.

As will be described later, even when multiplexing is not required by the system function, economic advantages can be achieved by using multiplexing since peripheral functions such as bandlimiting filters, clock drivers, the master clock, and other timing circuits can be shared between all of the multiplexed channels. CCD multiplexers are useful for multiplexing the outputs of arrays of detectors because they can operate with low signal levels and their performance improves at low temperatures where many detectors operate. CCD multiplexers are also useful in radar applications such as range gating (180) where radar returns from a single transmitted pulse are sampled at successive times. The samples are then clocked into the CCD device. If the clock is now stopped, the CCD stages will contain samples corresponding to the complete set of radar ranges and the individual stages corresponding to discrete radar ranges may be read out in parallel.

4.2.3. Recursive Filters. CCD's are perfectly suited for the implementation of a type or class of filter which contain a precisely controlled delay as an integral part of its construction. This class of filters consists of recursive and transversal filters. These types of filters are often erroneously called digital filters since until recently they were constructed using digital techniques.

Recursive filters are more flexible than transversal filters and form a more general class of filter because both feedback and feed-forward of the signals is used as shown in Figure 4.18 to shape the filter characteristics. The impulse response of a transversal filter is finite in time, whereas that of a recursive filter can theoretically be of infinite duration. Consequently, bandpass filters with sharp skirts can generally be designed with fewer arithmetic operations using recursive filtering than with transversal filtering. However, the recursive feedback amplifiers are very difficult to achieve on the same chip as the analog delay functions and are generally contained "off-chip" as separate components.

The following discussion of recursive filters follows closely that of Sequin and Tompsett (9). The transfer characteristic of an Nth-order

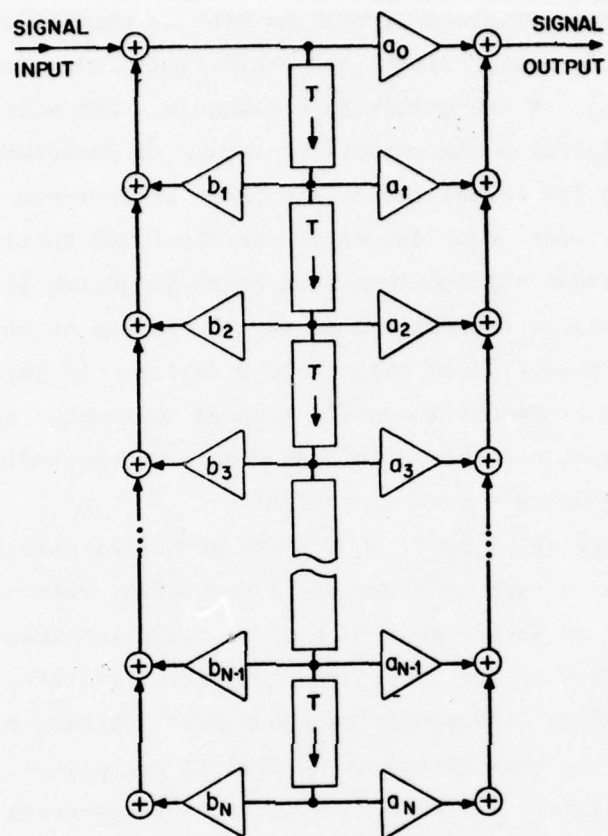


Figure 4.18. General form of the recursive filter indicating both feedback and feedforward of the delayed signal (after 9).

recursive filter in Z-transform notation is

$$H = (Z^{-1}) = \frac{\sum_{k=0}^N a_k Z^{-k}}{1 - \sum_{k=1}^N b_k Z^{-k}} \quad (4.6)$$

where the zeros and poles are generated by the roots of the polynomials in the numerator and denominator respectively. Transversal filters are obtained by setting all of the feedback coefficients b_k to zero.

A first order recursive filter is shown in Figure 4.19. This circuit provides positive feedback at all frequencies which are delayed by an odd integer multiple of one-half the signal period. Therefore, its transfer function shows a maximum at these frequencies and the circuit has the characteristics of a bandpass filter. For the case where the coefficient b_1 is greater than unity, the circuit becomes an oscillator since it is unstable.

Figure 4.20 shows a second-order recursive filter with a bandpass function, in which both the center frequency and bandwidth can be varied by changing the feedback coefficients (181,182). The response obtained with this circuit is shown in Fig. 4.21a for a 10 KHz clock. The two values of Q are obtained by varying b_1 and b_2 . Figure 4.21b shows the variation of the resonant frequency with the coefficient b_1 .

The second order filter performs similar to a normal tuned circuit and it is of interest to examine the filter parameters such as Q, center (resonant) frequency and bandwidth in terms of the attenuating constants b_1 and b_2 (181). Letting T represent time delay as indicated in Fig. 4.20, the transfer function of the circuit shown with $z = \exp(j\omega_s T)$ is

$$H(z) = \frac{a_0 z^2 + a_1 z}{z^2 - b_1 z - b_2} \quad (4.7)$$

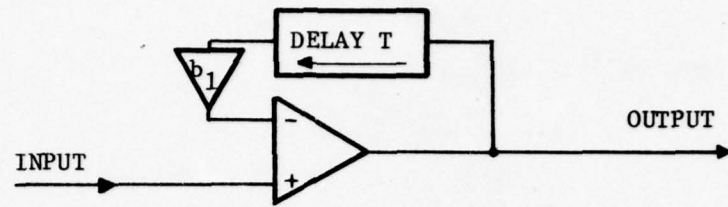


Figure 4.19. An example of a first order recursive filter (after 9).

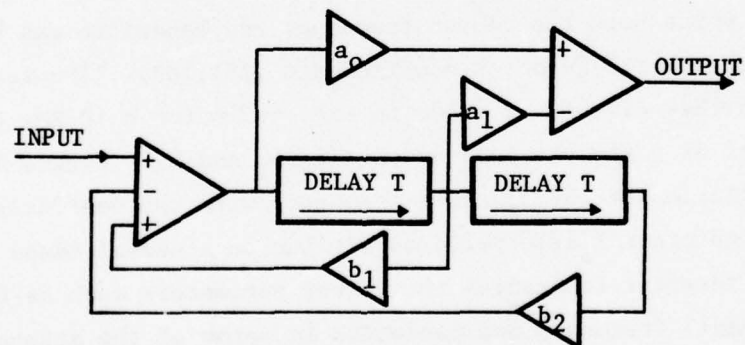


Figure 4.20. An example of a second order recursive filter (after 181).

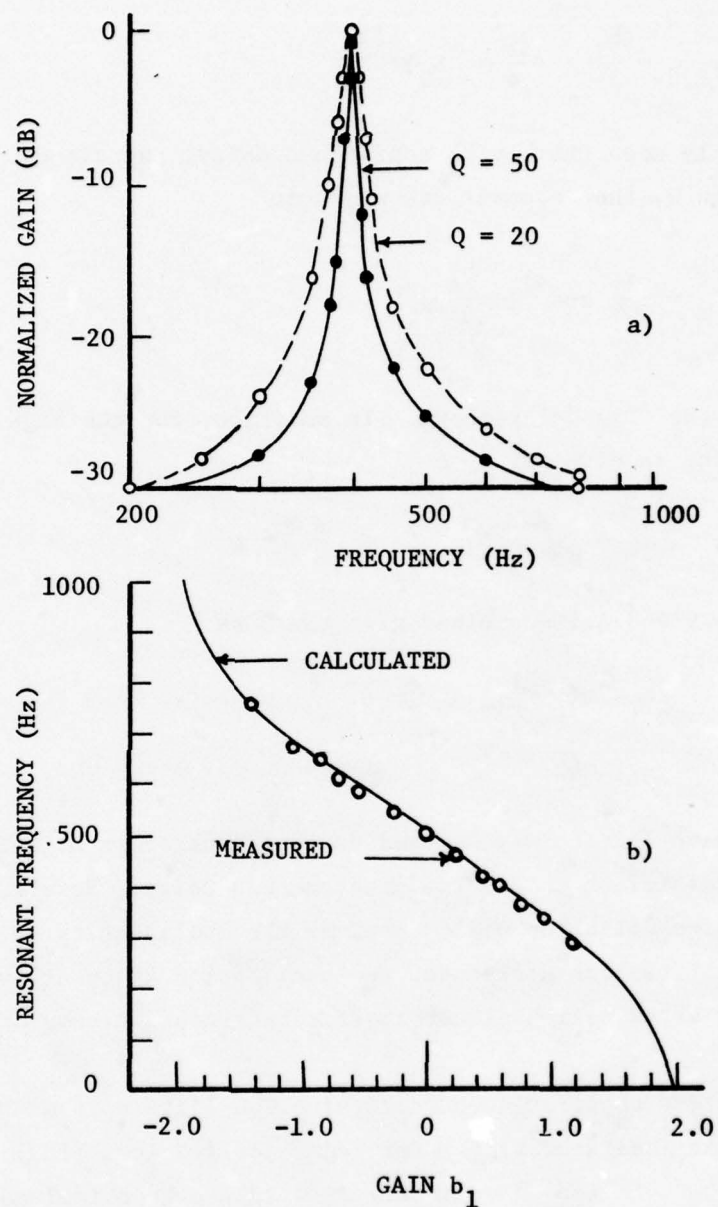


Figure 4.21. Measured results from two ten-stage charge transfer recursive filters: a) the amplitude response for fixed coefficients and b) the shift of the resonant frequency as a function of b_1 (after 181).

and the poles are located at

$$\gamma_{1,2} = \frac{b_1}{2} \pm \left(\frac{b_1^2}{4} - b_2 \right)^{1/2} \quad (4.8)$$

It is readily seen that as b_2 approaches unity, the circuit Q increases, and for high Q , the resonant frequency is

$$f_r = \frac{1}{2\pi T} \cos^{-1} \left(\frac{b_1}{2\sqrt{b_2}} \right) \quad (4.9)$$

where T is the time delay shown. In addition, for the high Q case, the 3db bandwidth is given by

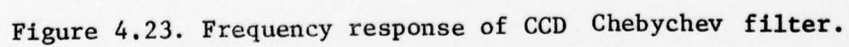
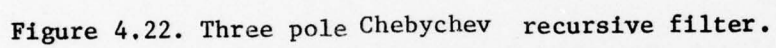
$$B = \frac{1}{\pi T} \left| \ln \sqrt{b_2} \right| \quad (4.10)$$

Equations 4.9 and 4.10 combined give the Q as

$$Q = \frac{\cos^{-1} \left(\frac{b_1}{2\sqrt{b_2}} \right)}{2 \left| \ln b_2 \right|} \quad (4.11)$$

Recursive filters may be used as tone generators by setting the feedback coefficient to a value greater than unity. However, since the frequency of oscillation will depend on the nonlinearity or clamping used to stabilize the amplitude, the oscillation frequency will require fine tuning by adjusting either the feedback coefficients or the clock frequency.

One recent application of recursive CCD filters is a Chebychev moving target indicator filter for radar applications (183). The three pole Chebychev filter shown in Figure 4.22 has been implemented using CCD delay elements. The numbers in Figure 4.22 refer to the coefficients at the inputs of the summing amplifiers. In this application, the summing amplifiers are 15 MHz bandwidth integrated circuit operational amplifiers.



An eight stage CCD was used for each delay.

Figure 4.23 shows the low frequency response of this filter with a swept frequency sine wave input. As shown in the figure, the response minima occur at 0,38.4 and 76.8 KHz. The filter output at the frequency minima is 32db down with respect to the maximum output.

Another recent study of recursive CCD filters was CCD recursive comb filters (184). In this study, high pass and low pass integrator filters and high and low pass canceller filters were treated both theoretically and experimentally. The implementation in each case used an 8-bit CCD as the delay element. The theoretical and measured characteristics of the high pass integrator comb filter are shown in Figure 4.24. As seen in this figure, comb filters are characterized by their periodic transfer characteristics in the frequency domain. As also shown in the figure, the agreement between theoretical and measured characteristics is excellent for this case. Other cases are also shown in the reference.

CCD recursive filters are somewhat more attractive from an economic standpoint if several channels are multiplexed through one filter. In this case more elements are required in the delay lines but the precision resistors and amplifiers are now time-shared. At any one time the only signal samples at the inputs or outputs of the recursive filter are those of one data channel and these are processed by the operational amplifiers at this time. The other samples are stored in delay lines and are processed in sequence as they are clocked through delay lines.

A second order recursive filter bank with 16 multiplexed channels has been demonstrated (185). This filter has the feedback and feed-forward coefficients stored in ROM's from which they are fed to multiplying D/A converters during the appropriate time slot for each signal channel.

In all known applications of CCD recursive filters, however, the feedback has been performed in off-chip operational amplifiers to obtain

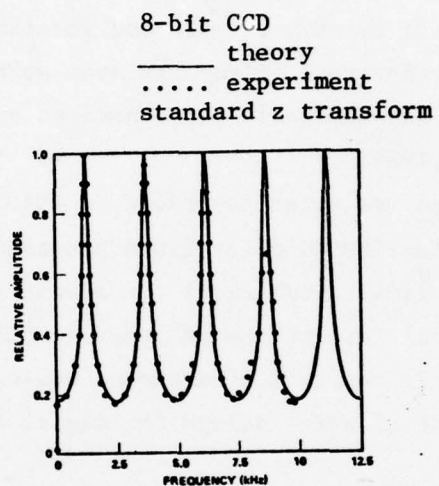


Figure 4.24. Highpass integrator CCD comb filter frequency characteristics (after 184).

the amplifier gain and phase stability required. For this reason, it is unlikely that CCD recursive filters will find wide acceptance until stable feedback amplifiers can be integrated on the CCD chip (180).

4.2.4. Transversal Filters. A significant number of charge-transfer devices have been developed for analog signal processing. The transversal filter, however, has special significance because it is a general purpose device in that any desired finite impulse response can be obtained with it as a function of the CCD delay line tap locations and weights. If the tap weights and locations can also be electrically varied, the transversal filter has even more significance, for the device can be automatically programmed to perform any linear-processing function (170,186).

The device was first described in 1940 (187) with either lumped constant or distributed delay lines proposed for the delay element, but has seen only limited use until the advent of CCD devices.

The general form of the transversal filter is shown in Figure 4.25 (9,186,188). It consists of a tapped analog delay line with N delay stages, D, each of which delays the signal by

$$T_c = 1/f_c \quad (4.12)$$

A sample exits from the last storage element NT_c seconds after it entered the circuit input. Each element h_k weights the output of its delay element and the circuit output is the sum of the N-weighted samples. This circuit therefore generated an output signal $v_{out}(t)$ which is the convolution of N weighted samples of the input signal $v_{in}(t)$. Therefore,

$$v_{out}(t) = \sum_{k=1}^N h_k v_{in}(t - kT_c) \quad (4.13)$$

Now to examine equation 4.13 in the frequency domain, assume an input of the form $v_{in}(t) = V \exp(j2\pi ft)$.

Equation 4.13 then becomes

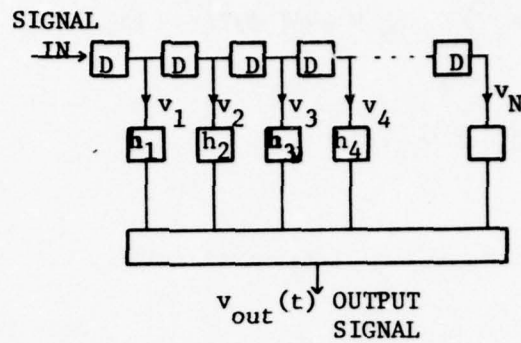


Figure 4.25. Block diagram of a transversal filter.

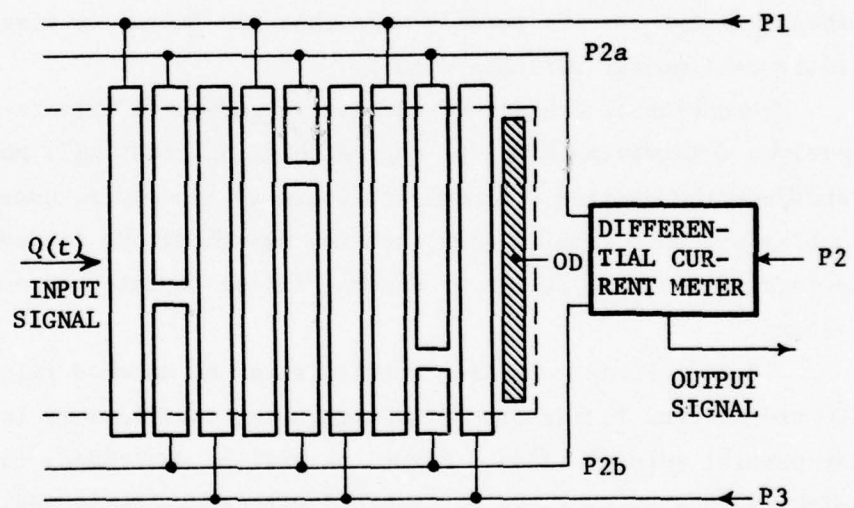


Figure 4.26. CCD transversal filter implementation using split electrodes to obtain the tap weights (after 188).

$$v_{out}(t) = \sum_{k=1}^N h_k v \exp[j2\pi f(t - kT_c)] \quad (4.14)$$

and after factoring out $v_{in}(t)$,

$$v_{out}(t) = v_{in}(t) \sum_{k=1}^N h_k \exp(-j2\pi f k T_c) \quad (4.15)$$

Therefore, the frequency response of the transversal filter is

$$\omega(f) = \sum_{k=1}^N h_k \exp(-j2\pi f k T_c) \quad (4.16)$$

Since $T_c = 1/f_c$, it is readily seen that the frequency response of the filter is linearly variable with f_c .

The design of frequency selective transversal filters primarily involves determining a set of tap weights, h_k , that will make $\omega(f)$ reproduce the desired frequency response as closely as possible. This problem has been studied (189) and the design of CCD transversal filters is identical to the design of digital finite impulse response (FIR) filters.

4.2.4.1. Fixed weighting coefficients and matched filters. The CCD transversal filter with fixed weighting coefficients is very attractive for several reasons (180). First, as will be described, the sampling, weighting and summing can be obtained with very little additional circuitry compared to the basic CCD shift register. Second, in a relatively small circuit, it replaces a large quantity of digital circuitry. Third, this function is required for a large number of important applications.

Fixed tap weight transversal filters are usually implemented using the split electrode approach in Figure 4.26. When the input signal

charge, $Q'(t)$, is transferred under the split electrodes, the charge packets will be balanced by an equal and opposite amount of charge on the split electrodes. The charge induced on the split electrodes, however, is also proportional to the area of each split electrode and in this way the tap weighting and summing operation is performed simultaneously. The total induced charge on lines P2a and P2b is then sensed by the differential current meter. (The charge induced in the split electrodes is also a function of the silicon substrate depletion layer capacitance, but for high resistivity substrates this is a second order effect and will be neglected in this discussion).

The weights, h_k , of each tap are obtained by designing the split electrode lengths in the ratio $(1 + h_k) : (1 - h_k)$ to produce the net weight of h_k at each node.

The split electrode dimensions and the resulting tap weights are determined by one mask in the integrated circuit process and this mask can usually be generated for less than \$500 (180).

A special implementation of transversal filters is the matched filter. A filter is said to be matched to a signal $V_s(t)$ when the impulse response of the filter $V_\delta(t)$ is the time reversal of the signal $V_s(t)$. Therefore (9),

$$V_\delta(t) = cV_s(\Delta - t) \quad (4.17)$$

where c and Δ are arbitrary constants. In the case of a tapped delay line,

$$V_\delta(kT_c) = h_k = cV_s(\Delta - kT_c) \quad (4.18)$$

The maximum response $V_o(kT_c)$, from the filter will occur at time $\Delta = NT_c$ after the signal to which it is matched is applied to the filter input. The output is given by

$$V_o(kT_c) = \sum_{k=1}^N h_k V_s(NT_c - kT_c) = 1/c \sum_{k=1}^N h_k^2 \quad (4.19)$$

In a matched filter, the components of the signal to be matched add coherently, whereas the output due to random noise will only be proportional to h_k (9). Therefore, the signal-to-noise ratio is proportional to the number of taps in the transversal filter. In the presence of additive white noise, this filter gives the best measurement of the signal amplitude or its arrival time.

Many examples of matched filters have been described. One of the earliest examples was a CCD matched filter used to detect a 13 bit Barker-coded p-n (binary) sequence (188). The 13 bit Barker code is (- - - - + + - - + = + -). The matched filter in this application resulted in a 13 to 1 improvement in signal-to-noise ratio over a single pulse signal method. This filter is simple to build since the tap weights have values of +1 and -1 and do not depend on the position of the split electrode placement.

Most applications of CCD transversal filters require analog tap weights and the split electrode technique can be used to implement any transversal filter function, i.e. low pass, bandpass or band reject. There are many good examples of CCD transversal filters in the literature (170,171,188,190-193). Figure 4.27 shows a photograph of a 63 tap low pass CCD transversal filter (190). The electrode splits are evident in the photograph and as seen in Figure 4.28 the measured impulse response of the filter has the same shape and was obtained by clocking a single charge packet along the device. The computed and measured low pass response of this filter are shown in Figure 4.29 and 4.30. This filter was designed so that with a 32 KHz clock, the maximum passband ripple was ± 0.1 dB between 0 and 3 KHz, and the stopband attenuation was 36 dB.

The accuracy of split electrode filters depends not only on the dimensional accuracy of the split but also on the depletion capacitance which is a function of substrate resistivity tolerance and variations in oxide thickness. An accuracy better than 0.5% of the maximum tap

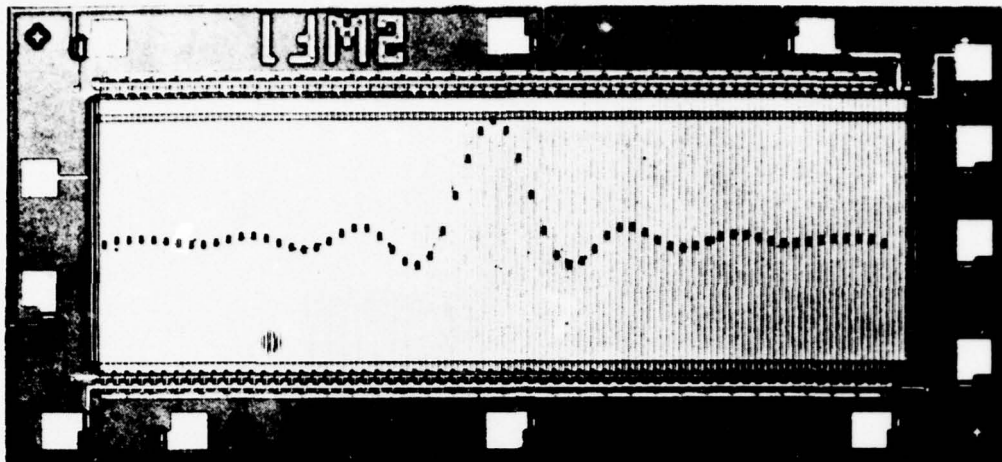


Figure 4.27. Photograph of CCD low pass transversal filter.

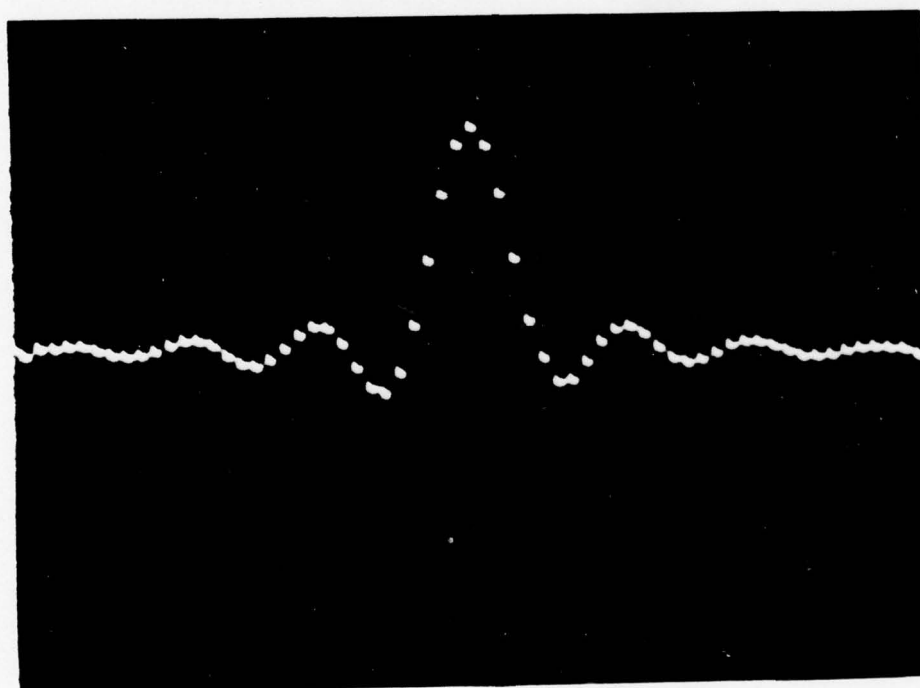


Figure 4.28. Measured impulse response of low pass filter.

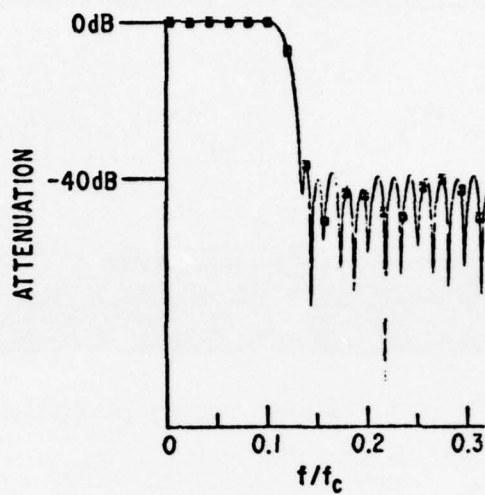


Figure 4.29. Computed response of 63 tap CCD low pass filter.

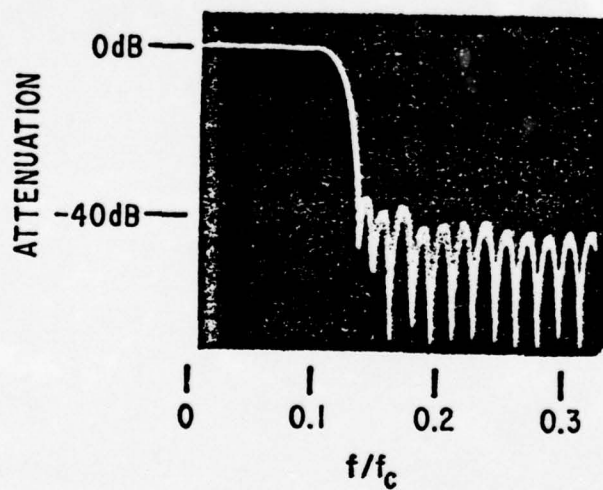


Figure 4.30. Measured response of 63 tap CCD low pass filter.

weight is required to obtain stopband attenuation of 40 dB. However, the tap weight error does not have a significant effect on matched filter functions because the input signal is contaminated with so much noise that the additional "noise" due to weighting error is negligible (180).

CCD's have also been used to perform the discrete Fourier transform (DFT) of a signal by means of the chirp z-transform (CzT). The transform is called the chirp z-transform because the mathematical operations involve multiplication and convolution with chirp (linear FM) signals (194). The DFT of a band limited electrical signal $g(t)$ is found by sampling the signal at N uniformly spaced instants of time to obtain the N points g_n . The DFT is then given by the definition (195)

$$G_n = \sum_{k=0}^{N-1} g_k \exp\left[-\frac{j2\pi kn}{N}\right] \quad (4.20)$$

The CzT algorithm for use with equation 4.20 is derived by making the substitution

$$2kn' = k^2 + n^2 / -(n - k)^2 \quad (4.21)$$

into equation 4.20 to obtain

$$G_n = \exp[-j\pi n^2/N] \sum_{k=0}^{N-1} g_k \exp[j\pi(n-k)^2/N] \exp[-j\pi k^2/N] \quad (4.22)$$

This equation represents the CzT algorithm and has three steps (9):

- 1) Premultiplication of the input samples g_k by a complex chirp waveform
- 2) Convolution in a filter having a complex chirp impulse response
- 3) Postmultiplication by a complex chirp waveform

The CzT algorithm is advantageous for CCD implementation because

the bulk of the computation is performed by a fixed weighting coefficient transversal filter. When only the power density spectrum is required, step 3 is replaced by a squaring operation and the resulting block diagram is shown in Figure 4.31.

Recent results on 500 point DFT devices have been presented (171,196). Two CCD filters were designed on a 160 x 100 mil chip. Each filter has 500 stages with one filter having sine weighting and the other cosine weighting. The results indicate that it is possible to successfully perform the discrete Fourier transform on one or two integrated circuits with the resulting low cost, small size and low power.

4.2.4.2. Adjustable tap weights. Many important analog signal processing functions require transversal filters with variable weighting coefficients and several methods are available or have been proposed for these applications (180). Variable tap weighting is more difficult and costly to achieve than fixed tap weighting. Therefore, the advantages of variable tap weighting CCD filters over more conventional digital approaches is not as obvious as is the fixed weight CCD filter case previously described.

It is relatively simple to design variable tap weights when the weights are binary values such as +1 and -1 or 1 and 0 as in the Barker code matched filter previously described. However, variable analog weights are much more difficult to achieve. The split electrode technique is not very amenable to variable weighting and other methods must be used. In general, these other methods consist of tapping the stages in the CCD device by adding sensing diffusions on the CCD stages or by using floating gates distributed along the CCD device. Both of those output techniques were discussed earlier in this report.

One approach to the variable weighting problem is the analog-binary approach (180) seen in Figure 4.32. In this case the analog weighting coefficients are digitized to M bit accuracy and the analog signal is clocked through M filters whose binary weighting coefficients

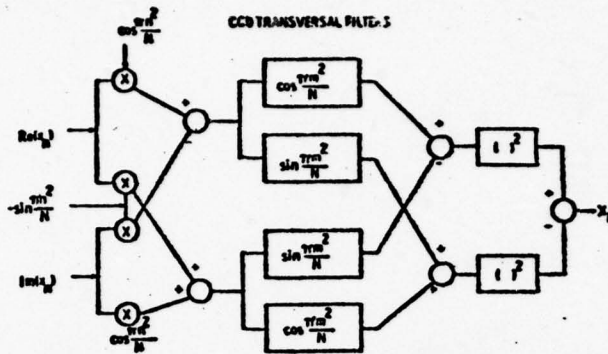


Figure 4.31. Block diagram of the implementation of the chirp-z transform using CCD's.

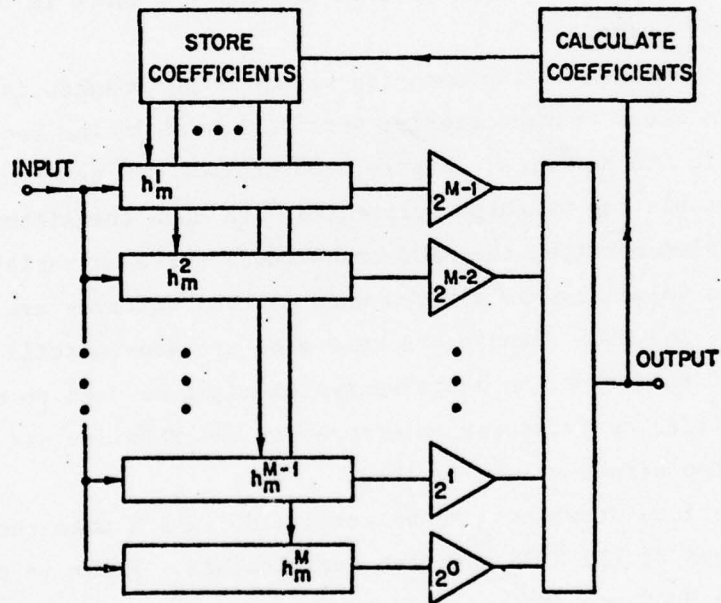


Figure 4.32. Variable tap weight transversal filter constructed from several filters with binary coefficients (after 180).

represent the desired filter response. If the h_k of equation 4.13 are written as

$$h_k = \sum_{m=1}^M h_k^m z^{M-m} \quad (4.23)$$

Then equation 4.13 becomes

$$v_{out}(t) = \sum_{m=1}^M \left[\sum_{k=1}^N h_k^m v_{in}[t - kT_c] \right] z^{M-m} \quad (4.24)$$

This technique is particularly effective in adaptive systems where the weighting coefficients can be stored as binary numbers in a memory for an indefinite time.

Another method of implementing variable tap weights is with MNOS transistors whose characteristics were discussed in the section on Non-Volatile CCD Memories. Figure 4.33 shows a CCD transversal filter with adjustable tap weights implemented with MNOS transistors (158). In this implementation, the MNOS transistors serve as variable resistors, whose values can be altered when control voltages are applied to the gates. The MNOS transistors here also are non-volatile devices. In a filter of this type an adaptive system might be used to overcome non-linearities or parameter tolerances in the MNOS devices and achieve the exact tap weight values desired.

Two serious drawbacks can be noted (180) which make the cost effectiveness of the MNOS approach questionable. First is the additional cost of the MNOS processing added to the existing complexity of CCD processing. Second is the off-chip circuitry required to program the MNOS transistors.

4.2.5. Correlators Correlation involves multiplying two analog

signals point by point and any of the adjustable tap weight transversal filters are potentially capable of performing this function. In this case, one of the analog signals would be loaded in the CCD delay line and the other signal would be used to vary the tap weights. However, as described in the previous section, this function is very difficult to accomplish. The full advantages of CCD's for correlation will be realized only when signals in two CCD shift registers can be multiplied in analog form on one chip, to obtain an all analog correlator (180).

A novel approach (197) which provides an interim solution to the above correlator problem is shown in Figure 4.34. Here, the analog signal charge packets are not clocked from cell to cell in the ordinary serial fashion. Instead, each signal charge packet is gated into a separate cell where it remains until it is replaced by a new signal sample. Non-destructive readout is accomplished by "sloshing" the charge back and forth within the 3 element cell and sensing the image charge induced in the overlying clock electrode. Since the charge packets move back and forth only within the confines of a single cell, the charge loss due to shifting is not cumulative as in a serial device. In this approach, although one of the correlation signals is stored in analog form, the other correlation signal can have only binary values (1 and 0 or +1 and -1). However, as will be explained, the device can be expanded.

The basic structure shown in Fig. 4.34 has an analog input bus which is scanned by the scan shift register to load the CCD cells with sequential analog samples of the input signal.

During the first part of the readout cycle, the sampled input of the charge is shifted to the center electrode site in each cell. The binary signal shift register then causes one of the two transfer gates per cell to cause the sampled signal charge to flow to one of the two output electrodes. In this way the correlation is performed in a manner similar to the binary Barker code matched filter described

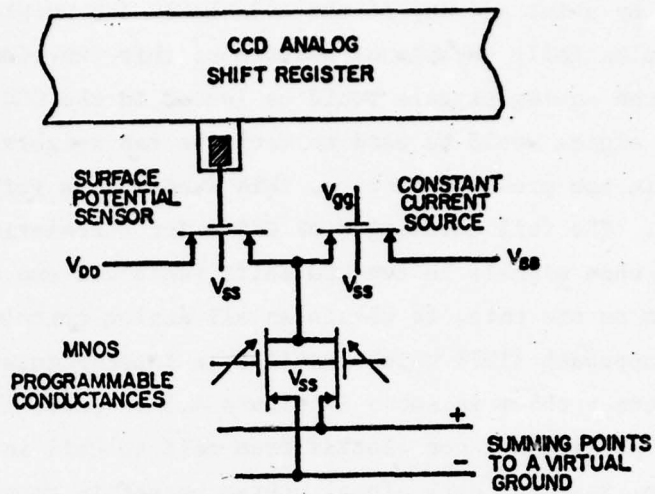


Figure 4.33. CCD transversal filter with non-volatile tap weights implemented with MNOS transistors (after 158),

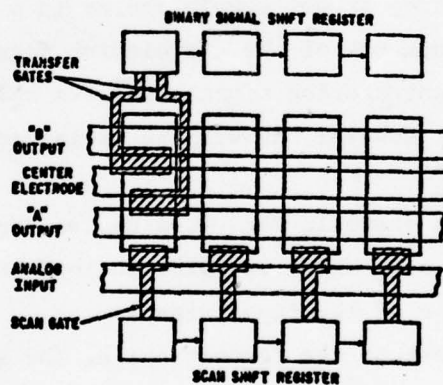


Figure 4.34. Layout of a CCD correlator using 3-element charge transfer cells and parallel charge transfer ("charge sloshing") (after 197),

earlier, except that now the transversal filter tap weights are variable in binary fashion under control of the binary signal shift register. The output signals from the A and B electrodes are applied to a differential amplifier to obtain the correlated output. This correlator technique has demonstrated a charge transfer loss of less than 10^{-7} per transfer and charge within a cell has been read more than 5×10^5 times without significant signal deterioration.

An extension of the simple correlator approach above may be made to handle a multiple bit binary word equivalent to one of the analog signals to be correlated. To accomplish this, several correlator chips are connected together so that the binary signals are passed from chip to chip. In addition the analog inputs of all chips are connected together and the output electrodes are also connected together. Since the analog samples remain fixed in position and only the digital signals propagated from stage to stage and from chip to chip, there is no degradation in signal accuracy as more chips are added.

4.3. Image Sensing

One of the most important applications of charge coupled devices is in solid-state image sensing. Like all other electronic image sensors, the CCD converts light quanta into charge that can be stored in a localized region and then read out in sequence. However, unlike present television camera tubes, it does not need the complex apparatus of a scanning electron beam in order to perform this function.

The features of CCD imagers that are superior to camera tubes are high signal to noise ratio, freedom from lag, and absence of microphonics. Additional benefits are small size, light weight, low power consumption, and precision image characteristics.

Charge is entered into the device via the absorption of photons near the potential wells, as opposed to the analog and digital signal modes where the charge is entered via an input voltage applied to a diffused source region. In imaging, charge is introduced into the device when light from a scene is focused on the surface of the device. As in all semiconductor devices, the absorption of light quanta creates hole-electron pairs which, under the influence of the potential beneath each storage electrode, are collected as charge packets. Thus, the quantity of charge stored at any storage site (pixel) is proportional to the intensity of the image at that site. In this manner, a spatial charge representation of the scene is stored in the device. It is transferred off the imaging device, to be used externally, when clock voltages are applied to the electrodes.

Solid-state image sensors can be divided into two categories - linear image sensors and area image sensors. Linear image sensors contain a single row of photosensitive sites and thus are basically one dimensional devices and can be used to monitor one dimensional variables such as the level of liquid in a tank or the diameter of a wire being fabricated (9). To obtain a two-dimensional output from a

linear sensor, the second dimension must be obtained by mechanical means such as a rotating mirror or the object being scanned must be moved in front of the sensor.

To obtain real-time images at the frame rate of standard television (30 frames/second), the image sensor must be electronically scanned in both directions (area image sensor). The primary problem with using a linear sensor with mechanical scan is that the image integration time per site is only one line time. Conventional electron beam scanned camera tubes integrate the charge during the entire frame time in order to obtain the image sensitivity required for room lighting conditions and the CCD imager must function in a similar manner in order to be competitive.

4.3.1. Linear Image Sensors. Linear imaging arrays can be organized in three basic ways (91). First, a simple CCD shift register can be used where the carriers are integrated in the transfer channel itself. While the charge is being integrated, the shift register clocks are stopped so that the charge can not transfer. During the subsequent readout, the clocks are turned on to read-out the integrated signal. The major problem with this approach is that the readout time must be short compared to the integration time in order to prevent smearing of the signal since the charge from the image is still integrating during the readout. A mechanical shutter could be utilized to prevent charge integration during readout, but in addition to the mechanical complexity of the shutter the integration time in this type of linear device is seriously shortened due to the relatively long serial readout time.

The solution to the above problem is to integrate an analog shift register beside the sensor sites (Figure 4.35). After integration in the sensors, the charge is shifted into the shift register through the lateral transfer electrodes. This lateral transfer can be accomplished in approximately one microsecond and the integrated charge can be shifted out while a new line is being integrated. This design virtually

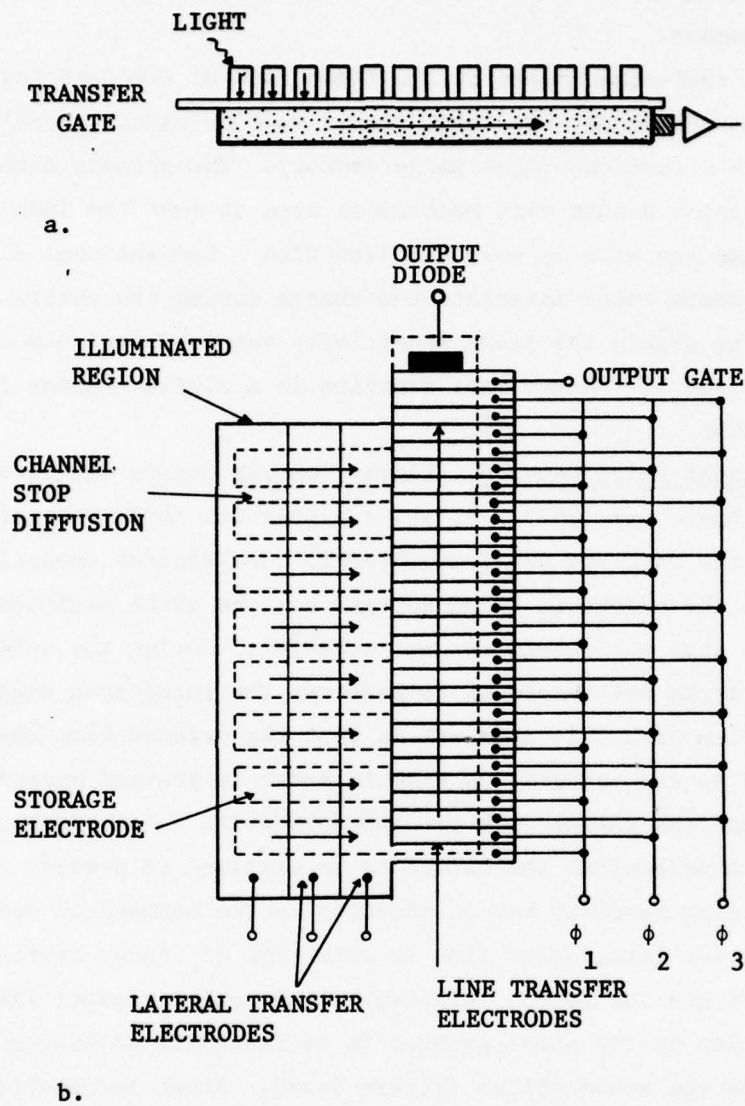


Figure 4.35. Linear CCD imaging array with single readout register, a) basic organization and b) detailed representation (after 9, 91).

eliminates the smearing problem and the integration duty cycle is nearly 100%. Normally the readout register in this type of device is shielded from the image to prevent the readout register from collecting image-induced charge and causing smearing. The maximum number of image sites which can be integrated into this structure is limited either by the maximum chip dimension or the transfer inefficiency in the readout register. Both of these limitations can be improved by using the double readout register (also called parallel-transfer (198) or bilinear (281) organization in Figure 4.36). This organization uses one line of sensors as before, but now incorporates two readout registers, which are shielded. After the integration is complete, the odd-numbered pixels are shifted into one readout register and even-numbered pixels are shifted into the other readout register. The information in the two readout registers is clocked into a two-bit register, thus reorganizing the pixels in the order in which they were formed in the image sites. The number of stages in each readout register is now one-half of the previous number. Therefore, the number of transfers required to shift any pixel out of the register is also one-half of the previous value. The layout packing density is also higher.

Linear arrays can be frontside illuminated if polysilicon, which is reasonably transparent in much of the visible and near-infrared spectrum, is used for gates. Figure 4.37 shows the spectral response versus wavelength for a 500 element frontside illuminated linear array. The peaks and valleys in the response curve are attributed to interference in the polysilicon and oxide layer boundaries. The spectral responsivity is defined as the signal current divided by the total radiant power (integrated over the entire blackbody spectrum) incident on the image area, including the area occluded by transfer gates. A photograph of this device is shown in Figure 4.38 and the double readout registers are clearly seen to the right and left of the central photosensor column. This device uses implanted bulk channels with 3-phase transfer electrodes selectively

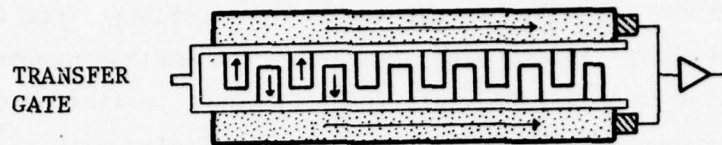


Figure 4.36, Linear CCD imaging array with double readout register (after 198).

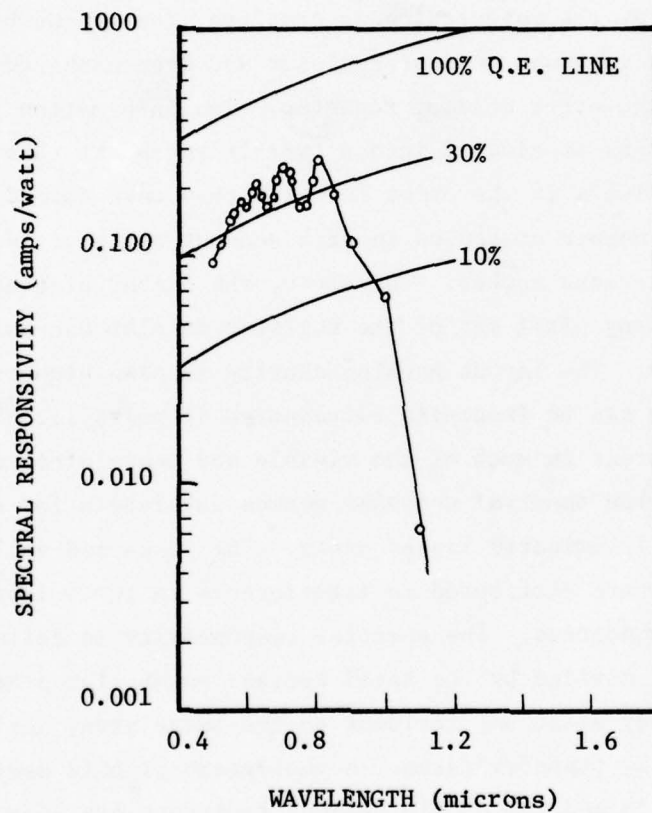


Figure 4.37. Spectral responsivity versus wavelength for frontside illuminated silicon gate linear array (after 199).

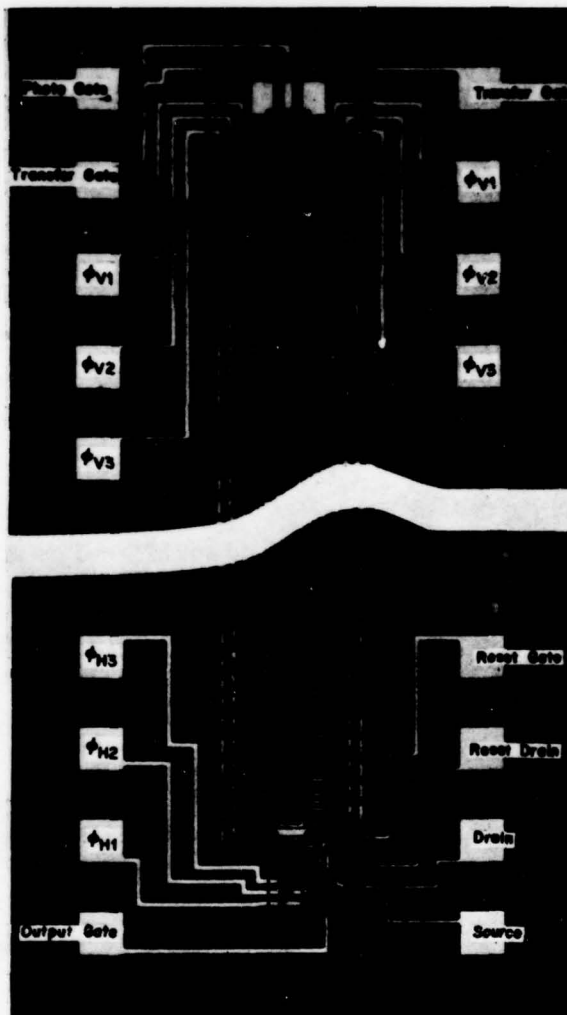


Figure 4.38. Photograph of a buried-channel CCD linear imaging array with 500 photoelements using double readout registers (after 199).

doped into a single layer of high resistivity polysilicon. The aluminum for the bus lines and bonding pads is also used to shield the shift registers from incident light. This device has very low noise and transfer inefficiency due to the bulk channel approach and has a dynamic range of about 3000:1. The image reproductions in Figure 4.39 illustrate the quality of this device. These pictures were taken in the slow scan mode at about one frame per second with the readout registers operating at 1 MHz. The light intensity variation shows that the picture remains clearly visible through two orders of magnitude of light intensity. In Figure 4.39d the graininess produced by noise has washed out the details of the picture.

A more recent example of a linear array is a 1728 element linear array (200) processed with a double level polysilicon, buried channel process. This circuit uses a single readout register. A CRT monitor display of the IEEE facsimile test charge generated by this device is shown in Figure 4.40. The image was horizontally scanned by the imaging device while vertical scanning was obtained by mechanical rotation of the test chart. A portion of this displayed image is also shown with an expanded monitor sweep. The maximum resolution obtained is 36 lines/mm.

The performance of this imaging array at low light levels is illustrated in Figure 4.41. This series of single frame photographs shows the display of approximately 700 photosites at illumination levels successively reduced from near saturation. For all of these photographs, the ambient temperature was 25°C and the clock rate was 1.5 MHz. The highlight area in Figure 4.41a represents an illumination of $200 \mu\text{W}/\text{cm}^2$ with a maximum charge per photosite of approximately 500,000 electrons. At a 1/1,000 reduction in light intensity in Figure 4.41d a fairly high quality image is retained although some dark current spikes appear as vertical streaks. At a 1/10,000 reduction in light intensity, the brightest area in the picture represents approximately 50 electrons/photosite, and it has been determined that the noise in this picture at



Figure 4.39. Pictures taken with a 500-element linear imaging device at four different illumination levels. The white signal level is close to saturation in a). The light levels in b), c), and d) are reduced by 10x 100x and 1000x from the levels in a) (after 146).



Figure 4.40. Picture of IEEE facsimile test chart from 1728 element linear imaging array (after 200).

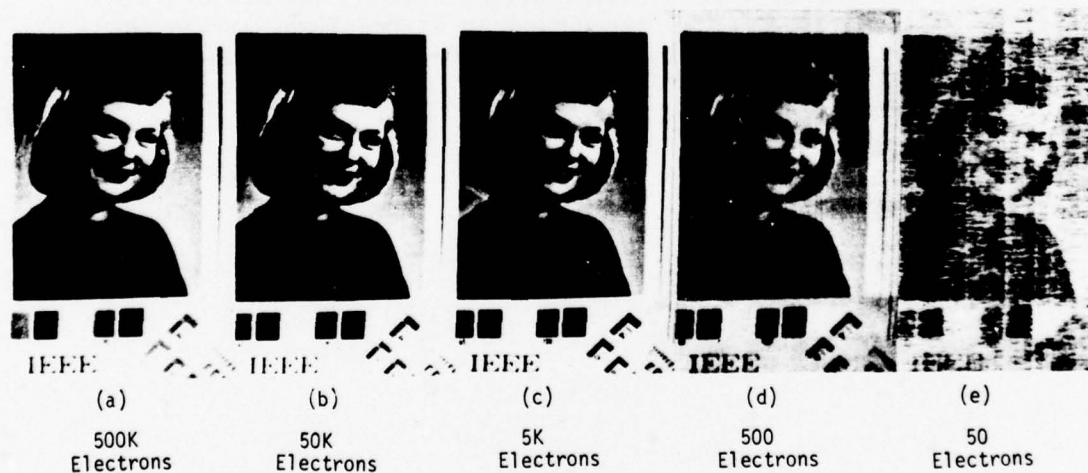


Figure 4.41. Imaging performance of 1728 element linear imaging array at different light levels (after 200).

this low light level is due primarily to noise in the amplifier.

It should be clear from these linear imaging array examples that CCD linear imaging arrays are well suited for slow scan applications such as facsimile where mechanical scanning is used in one dimension.

4.3.2. Area Image Sensors. 4.3.2.1. Imager organization. Area image sensors use the basic concepts developed for linear image sensors and essentially expand the sensor sites into an x-y or area matrix. It is obvious that in making this expansion from linear to area arrays, the problems encountered in fabricating the devices and in obtaining high and consistent performance have been compounded.

Several different concepts in technology and organization of area imagers have been developed and will be presented in this section. Figure 4.42 illustrates the basic readout organizations that may be used for area image sensors (9). The imager organization illustrated in Figure 4.42 is an x-y addressed organization used primarily for Charge Injection Device (CID) imagers. This device contains x and y address lines and each x-y coincidence point contains a pair of charge-coupled capacitors, which store the photon charge. Whenever the x and y address lines at a particular point are enabled, the integrated photon charge is injected into the substrate and the resulting signal is sensed on the address lines. The CID imager will be described in more detail later. Note that the CID device image sites are addressed in a manner similar to random-access memories used for binary data storage and the CID imager can also be randomly accessed if desired. The CID imager is usually not considered a true CCD device and in this paper the term "CCD" will not include CID devices, which will be described separately.

Area image sensors can be made by collecting basic linear image sensors in parallel rows on one chip to form a two dimensional array (line transfer organization). Figure 4.42b illustrates this concept with a readout register provided to read out the signal in the vertical

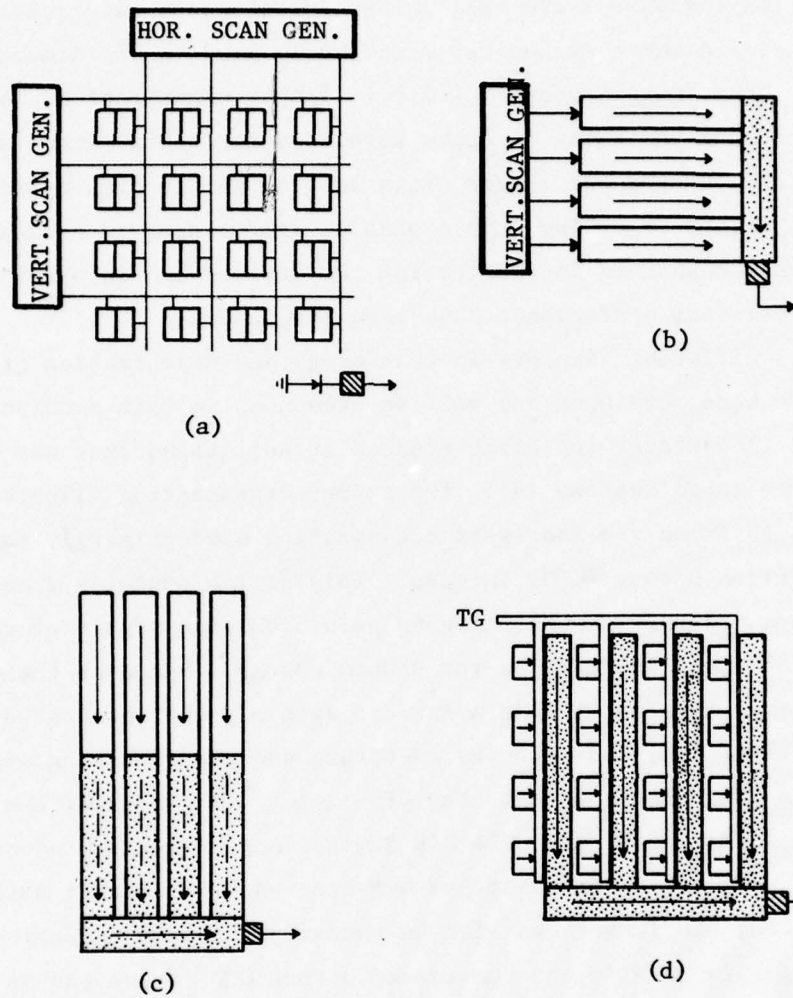


Figure 4.42. Readout organizations of area image sensors: a) x-y addressed charge injection device, b) line addressed organization, c) frame-transfer organization, d) interline-transfer (after 9).

direction. The difficulty of this organization is that the read out of each line has to be started with the proper timing, since there is a variable delay from each scanner row to the register output.

An improved approach is shown in Figure 4.42c where the image array is duplicated in a signal storage area with the same number of elements as the image array (frame transfer organization). During the vertical retrace time in a television display system, the image charge stored in the image array is quickly shifted down into the signal storage array. The image is now stored in the signal storage array and the image array is returned to the image integrating mode. During the horizontal retrace time, the stored signal is shifted down one bit so the bottom row of the charge is shifted into the output register. During the next horizontal line time, this charge is shifted out to form the video signal. Although this organization does have the disadvantage of requiring increased signal storage area, this disadvantage is compensated by the simplicity of the imager electrode structure and compact image storage and transfer cells.

Another important organization to be considered is the vertical interline-transfer method in Figure 4.42d. In this organization, the imaging and storage functions are integrated within the same area and the frame transfer occurs in a single step. Charge is accumulated in the imager sites while the signal from the previous field is shifted in the vertical signal storage channels in a manner similar to that used in the frame transfer organization.

The simpler operation of the vertical interline transfer method must be weighted against the more complex cell design as compared with the frame transfer approach, and the reduction of the image integrating area since the signal storage area must be light-shielded. Also, the vertical interline transfer method cannot be used with backside illumination since the shielding of the signal storage area is not practical.

Broadcast and closed circuit television systems reduce the visible

flicker of the image by using a 2:1 interlaced format where two fields occurring at a 50 or 60 Hz rate are alternately superimposed to obtain a 25 or 30 Hz frame rate. The odd lines of the frame are displayed in the first field and the even lines are displayed between the odd lines during the second field. To be compatible with the standard systems, solid-state imagers must also incorporate interlace provisions.

In the line transfer organization, the number of horizontal imager channels would be equal to the number of display lines in a frame (87). In vertical frame-transfer structures, the total number of cells can be reduced by a factor of 2, since the number of rows need only equal the number of display lines within a field rather than within a frame. The video signal for the second interlaced field can be obtained by electronically shifting the center of each integration site by half a cell. In 2-phase devices this is easily accomplished by forming the integrating potential wells alternately under the phase 1 or phase 2 electrodes. In 3-phase structures interlacing can still be accomplished by using combinations of phase 1, 2 and 3 electrodes but the technique is more complicated than in 2-phase structures.

The interline transfer method can also share vertical transfer cells between two fields but twice as many separate storage sites are associated with each register. Only half of the storage sites are read out in each field.

4.3.2.2. Examples of area image sensors. Examples of area image arrays will now be described. The first is a 128 row device with 220 elements per row processed with a three level polysilicon gate process (201). The device uses the frame transfer (FT) principle and is designed to fit the timing requirements of the PICTUREPHONE system. Since the total field time in this system is $133 \frac{1}{2}$ lines, $5 \frac{1}{2}$ lines times are available to accomplish the frame transfer. The photogenerated charge is integrated alternately under different sets of electrodes to provide the 2:1 interlaced format of this system. A video

element rate of 2 MHz was chosen so that horizontal resolution would match vertical resolution.

A schematic layout of this device is shown in Figure 4.43. The horizontal center-to-center spacing of the vertical transfer channels is 30 μm . These channels stopping diffusion (CHANSTOP). This results in an electrode length of 10 μm in the readout register. The interlace and 11:10 aspect ratio of the PICTUREPHONE screen now dictates a cell length of 48 μm in the imaging area and an active electrode length of 16 μm . Image size requirements do not dictate the size of elements in the storage area and the electrode are made 10 μm long. The mutual overlap of adjacent electrodes has been made 2 μm .

The overflow drains (OV) are interconnected at the upper end of the device by a diffused bus line (IOD). This bus line can serve as an input diode and in conjunction with the two input gates (PGL, PG2) can provide background charge injection to improve transfer efficiency in the vertical transfer channels.

The serial output register ends in an output gate (OG) and an output diode (OD), which is connected to the gate of a MOS amplifier. After the signal has been sensed between source and drain (AS, AD), the charge packet is discharged through a dump gate (DG) into the dump diode (DD).

The multiple reflections of the various interfaces in this device cause wavelength dependent interferences which result in a highly structured transmission curve. Therefore, the response curve of the device shows several peaks and valleys throughout the visible spectrum. Figure 4.44 shows the spectrum of two devices shown as curves A and B, from two different processing batches. The differences in these curves are attributed to differences in the thickness of the polysilicon layers. Curves A and A' were obtained from the same device with A' near the edge of the device and A in the center. The lowest spectral sensitivity in these devices is observed in the blue range and

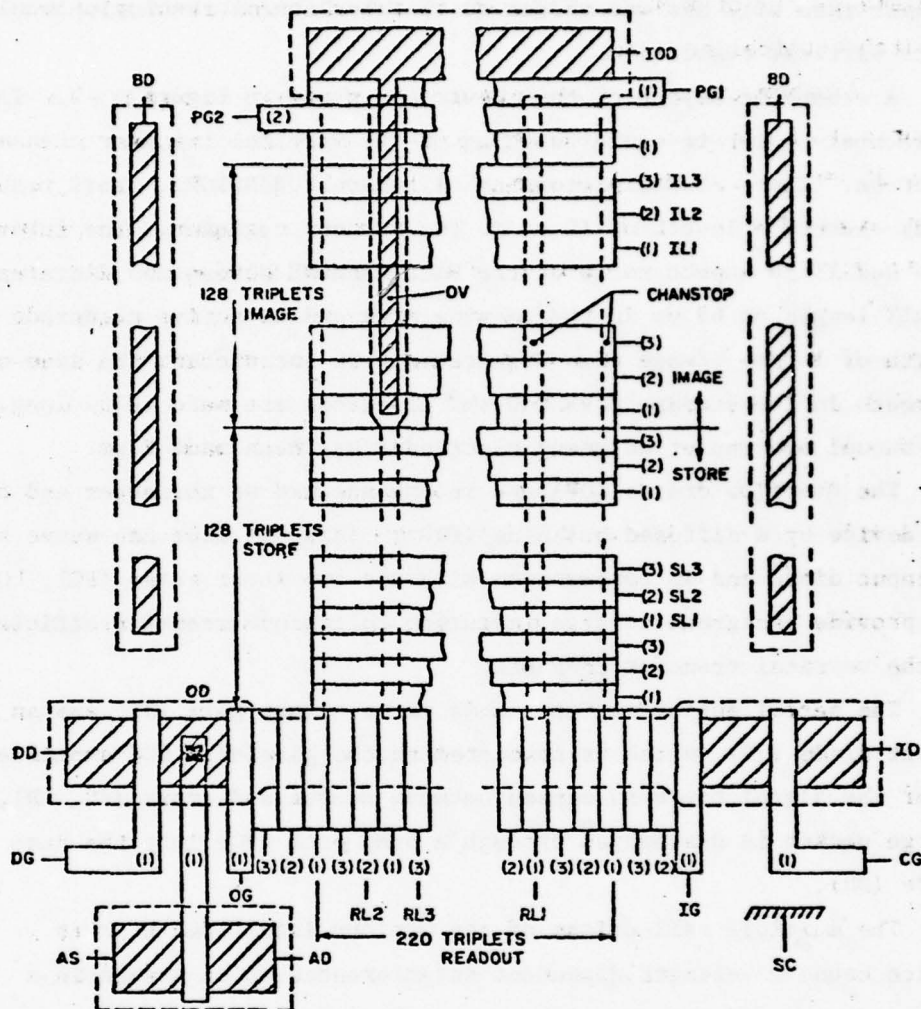


Figure 4.43. Schematic layout of 128 rows (256 element) by 220 elements per row area image sensor. Diffusions are hatched. Electrode levels are indicated by numbers in parentheses (1), (2) or (3). (after 201).

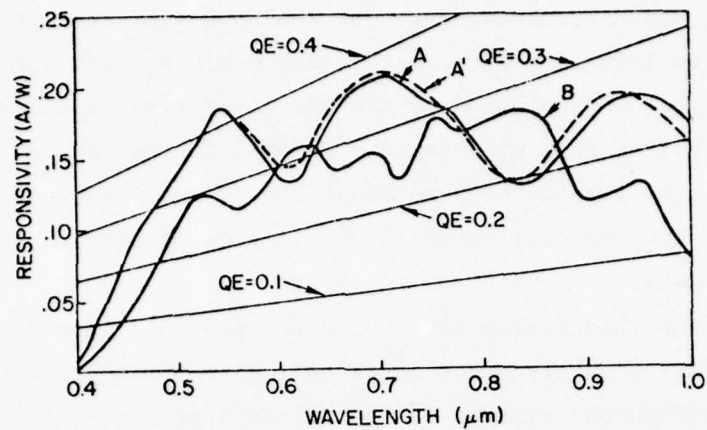


Figure 4.44. Example of the spectral response curve of two 256 by 220 element devices. Curves of constant quantum efficiency are included for comparison (after 201).



Figure 4.45. Monitor images obtained with the 256 by 220 element imager (after 201).

this, plus the nonuniform response over the spectrum, will present a problem when building a color camera. For optimum black and white television and for color systems, where the interferences in the spectral range of interest will cause problems, the device could be thinned down in the imaging area to about 20 μm , and illuminated on the back side. The spectral response should then be comparable to diode array targets.

References on this device have not discussed the blooming properties of the array, probably since antiblooming requirements in image sensors for PICTUREPHONE systems are much less stringent than for general purpose imager applications.

Monitor images obtained from this device are shown in Figure 4.45. The device was operated inside a small self-contained battery-operated camera which consumes only 1.5 watts.

The second area imager to be described is a 190 x 244 element device (202). This device is processed with a 2 level polysilicon gate, buried channel n-channel process. The device uses the interline transfer system and is designed for front side illumination. It has 190 columns of 244 elements each, alternating with optically insensitive vertical shift registers. A larger device with 380 columns of 488 elements is being designed by the same manufacturer for full frame NTSC TV compatible performance.

The schematic layout of this device is shown in Figure 4.46. The optically sensitive area of the array, detailed in Figure 4.47, has an aspect ratio of 4:3. The photoelement cell size is 14 μm by 18 μm with 4 μm of vertical overlap in the channel stop and 16 μm of horizontal separation due to the interleaved vertical shift registers. The output signal format provides two interlaced fields of information in the conventional left to right, top to bottom TV sequence. Two output amplifiers are provided in this design. A single stage floating gate amplifier (SFGA) provides an output level of 300 mV into an

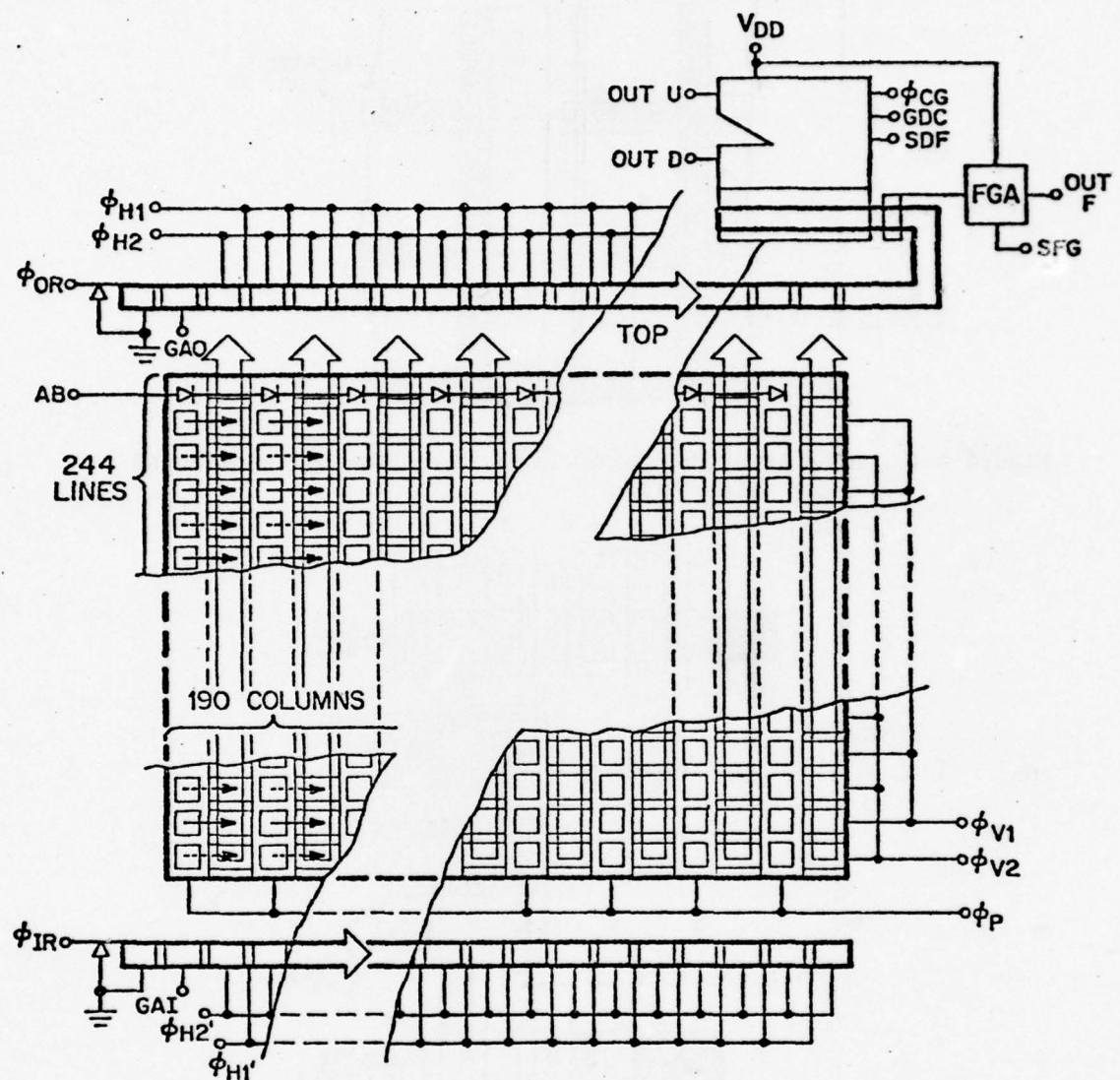


Figure 4.46. Schematic layout of 190 by 244 element area imaging array (after 202).

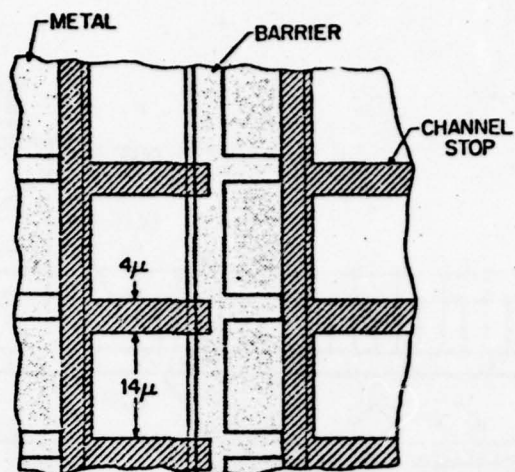


Figure 4.47. Area array detail of 190 x 244 element area imaging array (after 202).

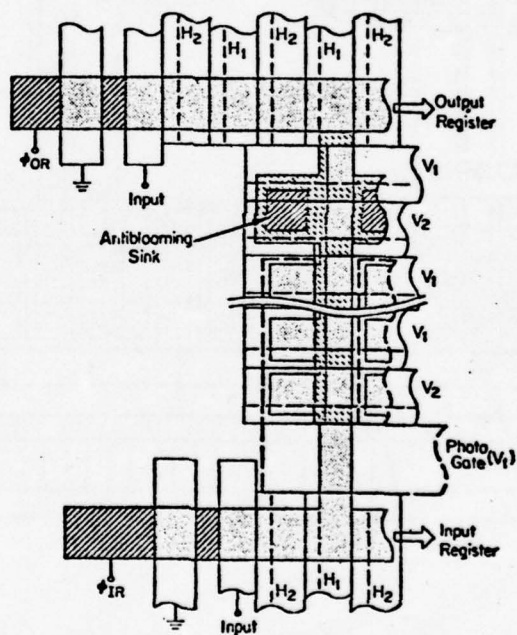


Figure 4.48. Blooming suppression structure (after 202).

510 ohm load for near saturation level signals at the 7.16 MHz data rate. The floating gate amplifier design was chosen because it provides a video signal free from reset noise and operates with a random noise level of less than 100 electrons. A twelve state distributed floating gate amplifier (DFGA) is also provided for very low light level applications. The DFGA has two outputs, one of which is delayed from the other by one-half a horizontal clock period. By summing these outputs off chip, clock voltage components in the video output are cancelled.

A column antiblooming technique has been applied in this design. The purpose of the antiblooming structure is to prevent excess carriers generated by overexposure of one or more photosites in a column from spreading to adjacent columns. A sink for excess carriers is provided at the top and bottom of each vertical shift register, as shown in Figure 4.48. At the top, above the last photosite, between the horizontal output register and the area array, a line of n^+ regions is diffused into the structure. These n^+ carrier sinks are electrically separated from the vertical shift register by a barrier. The n^+ regions are connected together by metalization and connected to the antiblooming terminal. When an appropriate positive bias is applied to the antiblooming terminal, any carriers exceeding the barrier potential will be removed before they can reach the horizontal output register, where lateral spreading would occur. At the bottom of each column, the horizontal input register, properly biased, provides a similar sink. In Figure 4 49, the device performance with and without blooming suppression is compared. The intensity of a light spot approximately six elements wide was varied from near saturation to 10^3 times saturation and 1.6×10^4 saturation. At 10^3 times saturation, severe image degradation occurred over the entire picture area without blooming suppression; with antiblooming bias applied, the image degradation was limited to about 10% of the picture area. At

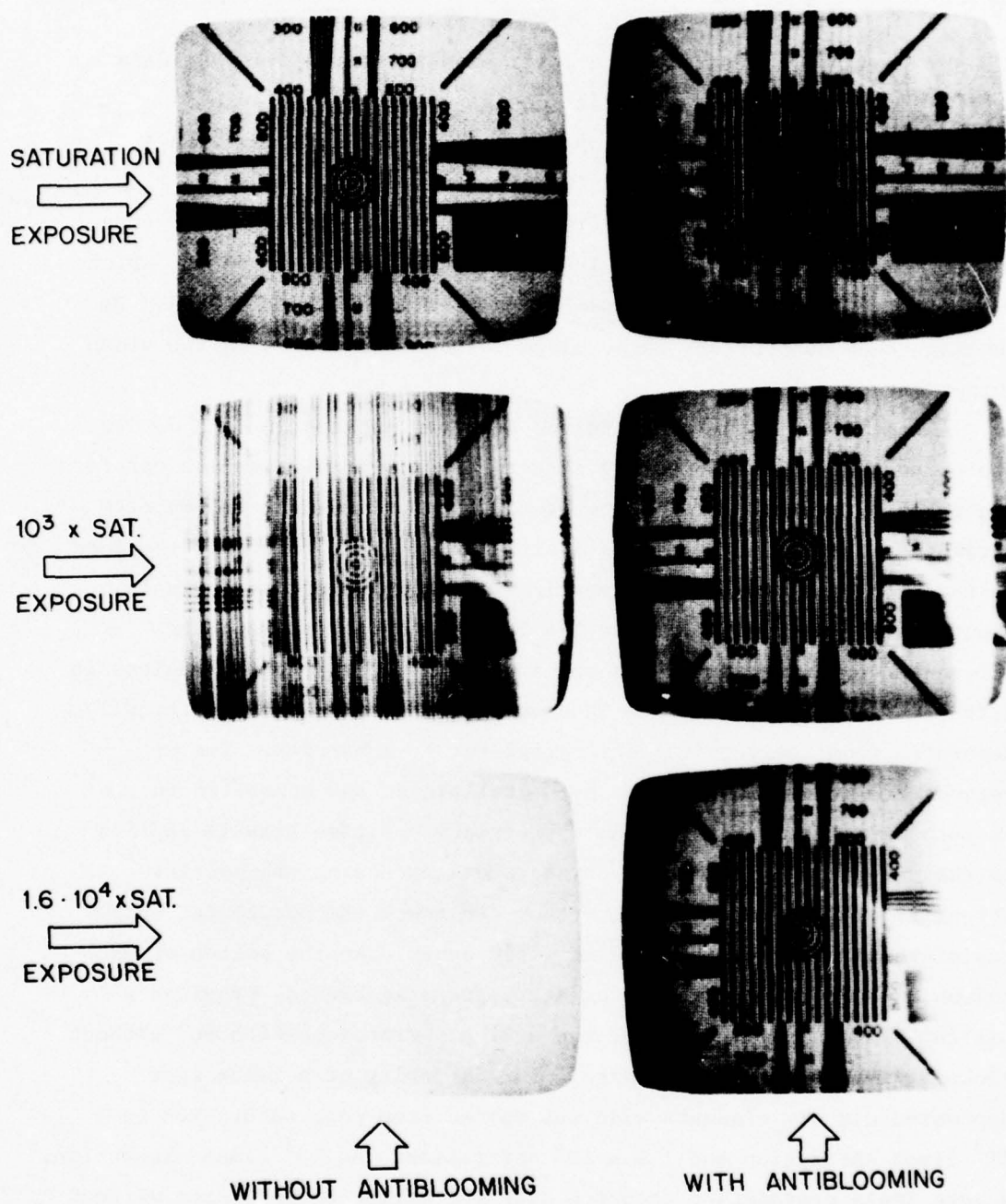


Figure 4.49. Blooming suppression characteristics (after 202).

1.6×10^4 times saturation exposure, the device was completely flooded without antiblooming while 75% of the image remained unaffected with antiblooming.

Room temperature and cool temperature measurements have been made, using the DFGA output. Figure 4.50 shows images obtained at -10°C for signal levels ranging from near saturation to 25 electron highlight charge packets (202). Equivalent images at room temperature required about twice as much signal charge as required at -15°C . The signal level in the 25 electron image in Figure 4.50G is less than the noise equivalent signal.

The third device to be described is a 512×320 element area image sensor (203, 204) that generates standard 525 line TV pictures. This device uses a single layer doped polysilicon gate structure. The individual gates are formed by doping n^+ regions in a p -layer of polysilicon on top of the channel oxide. Since there are no exposed gaps, a stable sealed channel structure results. An n -channel process is used for high speed performance and surface channel operation is used because it has the largest signal handling capability and has exhibited lower dark currents and dark current spikes than buried channel devices. Surface channel operation was also chosen because of its ability to control blooming by operation in the accumulation mode (205, 206).

Vertical frame transfer is used because it can be implemented with no biasing (small details in the scene do not contribute to the output due to obscuration), and it allows interlaced operation with complete readout in one field. The image area and storage area each contain 256×320 cells. The image area is interlaced 2:1 to create a 512×320 element picture.

Typical performance results with interlaced non-blooming operation are shown in Figure 4.51. Figure 4.52 shows a standard interlaced 525 line picture made by the 512×320 element device.

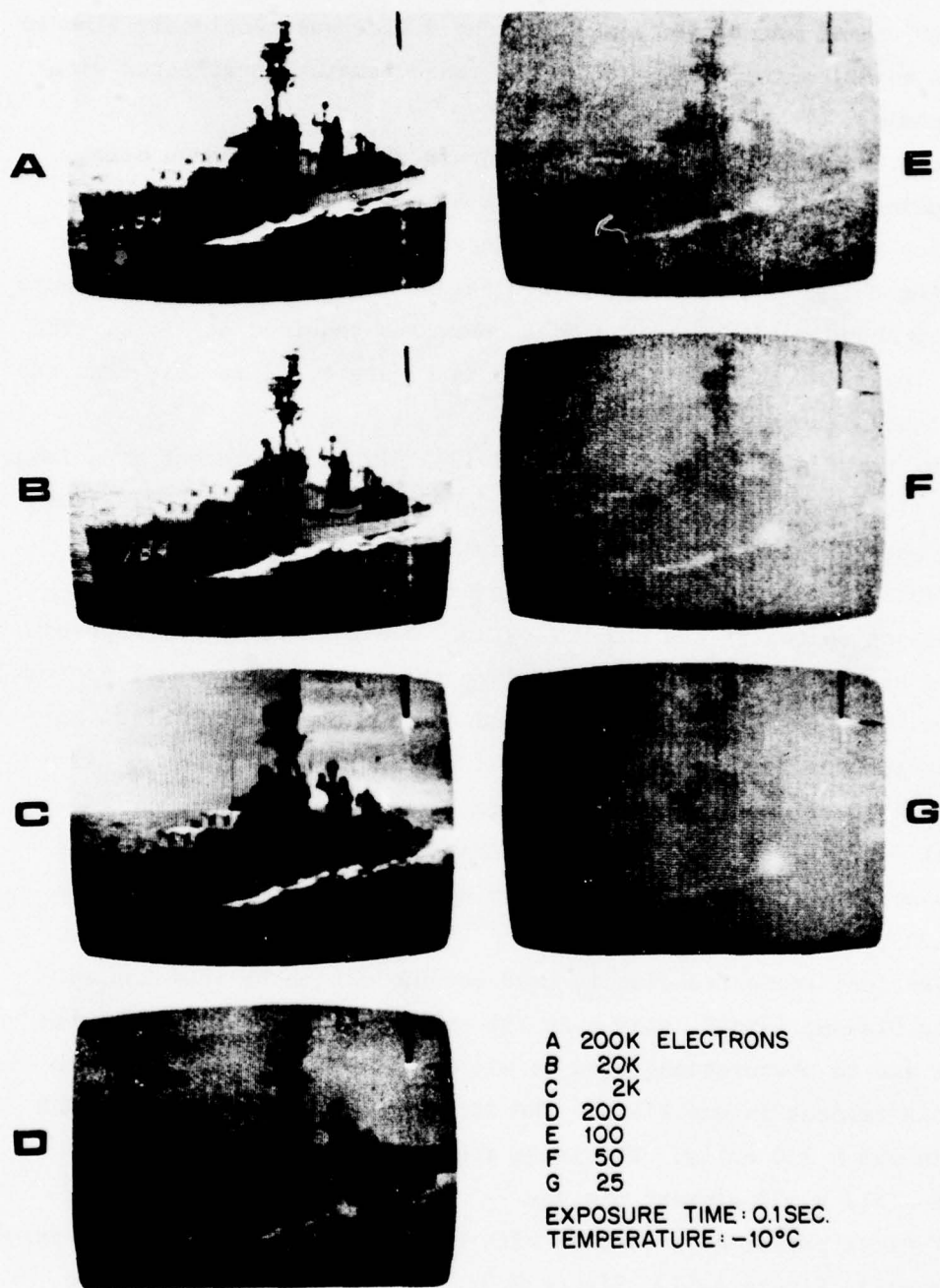


Figure 4.50. Low light level performance (after 202).

Typical Performance Data

Conditions: Standard EIA RS-170 525-line TV format operating at 25° C.

Electrical

Parameter		Unit	Note
Horizontal Clock Rate	6.1	MHz	
Video Bandwidth	3.0	MHz	
Vertical Transfer Rate	0.23	MHz	
Light Integration Time	16.67	ms	
Image Area Dark Current	4	nA	1
Image Area Light Bias Current	30	nA	1
Peak-to-Peak Signal Current	250	nA	1
Peak-to-Peak Signal Voltage	12.5	mV	2
Saturation Peak-to-Peak Signal Current	400	nA	1
Horizontal Register Bias Current	300	nA	1
Horizontal Limiting Resolution	240	TVL/PH	3
Vertical Limiting Resolution	480	TVL/PH	3
Contrast Transfer Function (CTF)	0.4	—	4
Gamma	1	—	5
Signal-to-Noise Ratio	50	dB	6

Optical

Sensitivity (Luminous)	3250	μA/lm	1,7
Sensitivity (Radiant)	65	mA/W-2856 K	1,7
Faceplate Illumination (250 nA signal)	0.1	fc	7

Notes

1. DC current from image area measured at RD.
 2. Developed across 3 kilohm load resistor at OS.
 3. Observed with EIA Resolution Chart and good quality monitor.
 4. Measured at 200 TVL/PH with an infrared blocking filter (2 mm HA-11).
 5. Measured between 4 and 400 nA signal current.
 6. Video peak signal (250 nA DC) to RMS noise.
 7. Measured with 2856 K illumination.
-

Figure 4.51. Typical performance results of a 512 by 320 element imager (after 203).



Figure 4.52. Standard 525 line picture generated by the 512 x 320 element device (after 203).

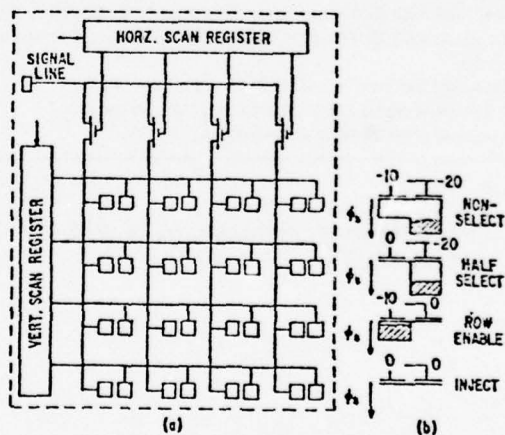


Figure 4.53. Basic CID device, a) schematic diagram of array, b) sensing site cross-section showing silicon surface potentials and charge locations (after 207).

Although the charge injection device (CID) is not a true charge coupled device in the sense in which the term has been used in this report, its basic operation does depend on charge transfer. Also, the CID device has demonstrated very significant results and represents a commercially available alternative to true CCD's for image sensing applications.

In contrast to CCD imagers, in which the signal charge is transferred to the edge of the array for sensing, the CID device confines the signal charge to the image collection site during sensing (206-208). Site addressing is done by an X-Y, coincident voltage technique, similar to that used for random access digital memories. Therefore, the device is not a basic serial access device as are all the CCD devices discussed here, but is instead a true parallel or random access device.

The basic CID device schematic diagram is shown in Figure 4.53 with its integral scanning shift registers. Each sensing site consists of two MOS capacitors with their surface inversion regions coupled such that charge can easily transfer between the two storage regions at each imaging site. A large voltage is applied to the row-connected electrodes so that photon-generated charge collected at each site is stored under the row electrode. The sensing site cross-sections in Figure 4.53 illustrate the silicon surface potentials and locations of stored charge under various applied voltage conditions.

A line is selected for readout by setting the line voltage to zero by means of the vertical scan register. Signal charge at all the sites in that line is transferred to the column capacitors, depicted by the Row Enable condition in Figure 4.53b. The charge is then injected by setting each column voltage to zero, normally in sequence, by way of the horizontal scan register. The video signal can be detected in the substrate, the driver circuit or the driven array lines. Usually, the array lines provide the lowest capacitance environment for signal detection. The half-select condition in Figure 4.53b

describes the charge condition in the unselected lines. This injection and readout technique has been termed the sequential injection method.

The "parallel injection" method was subsequently developed and will now be described (207, 208). In this readout method, the functions of signal charge detection and injection are separated. The signal charge at each sensing site is detected by intracell transfer during a line scan and the charge in the selected line can be injected during the line retrace interval. A diagram of a 4 x 4 site array similar to the sequential injection diagram but designed for parallel injection, is shown in Figure 4.54. At the beginning of a line scan, all rows have voltage applied and the column lines are reset to a reference voltage, V_s , by means of switches S_1 through S_4 , and then disconnected so that the column lines float. Voltage is removed from the horizontal line selected for readout (X3 in the example), causing the signal charge at all sites in that line to transfer to the column electrodes. Due to this action, the voltage on each floating column line changes by an amount equal to the signal charge divided by the column capacitance. The horizontal scanning register is then operated to scan all column voltages and deliver the video signal to the on-chip video amplifier.

At the end of each line scan, all the charge in the selected line can be injected simultaneously by driving all column voltages to zero with switches S_1 through S_4 . As an alternative, the injection operation can be omitted and voltage reapplied to the row after readout, causing the signal charge to transfer back under the row electrode. This operation is therefore a non-destructive readout.

The parallel injection approach permits high speed readout and is compatible with TV scan formats. A 244 line by 248 element imager employing the parallel injection technique and including an on-chip preamplifier, has been designed and fabricated with a p-channel, silicon gate process, modified to provide a top contact to the epitaxial layer. The image shown in Figure 4.55 was produced by the

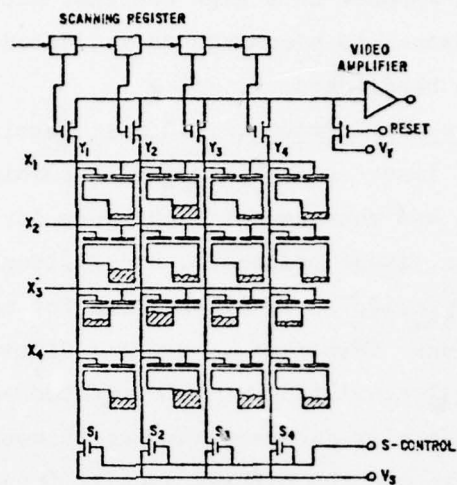


Figure 4.54. Schematic diagram of a CID array designed for parallel injection readout (after 207).

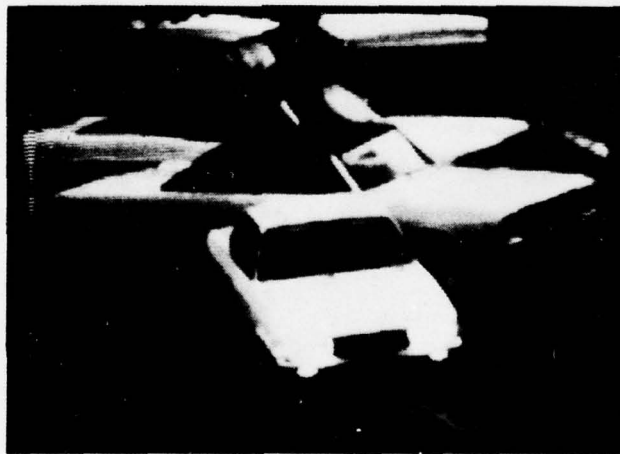


Figure 4.55. Image obtained from 244 x 248 site CID imager (after 207).

244 x 248 site imager exposed to a high contrast scene. Note that the imager is highly resistant to blooming, as indicated by the image of the bright automobile headlights.

4.3.3. Image Array Performance. 4.3.3.1. Resolution. One important property of image sensors is spatial resolution. The theory of spatial resolution and measurement techniques for conventional tube type imagers (vidicons, image orthocons, and silicon diode arrays) are well established and provide an excellent base for comparison of CCD imagers. The raster-scan format of TV systems dictates that the horizontal and vertical resolution must be treated separately. A solid state imager takes spatially discrete samples in both dimensions. The Nyquist theorem states that the highest spatial frequency which can be resolved is equal to one-half the spatial sampling frequency given by the periodicity of the integration sites (9). If images with spatial frequencies above the Nyquist limit are projected onto an image sensor, those frequencies will appear reflected back into the baseband. This results in aliasing or Moire effects. This is analogous to the situation of Brillouin Zones in periodic crystal structures (209).

An important parameter in defining imager resolution is Modulation Transfer Function (MTF). The MTF is the ratio of device output to device input in a particular observation domain (210). In the frequency domain, the MTF relates the amplitude and phase of a sinusoidal output to the corresponding sinusoidal input signal. In the case of a linear system, the MTF is the Fourier transform of the impulse response function.

The MTF for a CCD imager is the product of functions accounting for the signal degradation due to thin film surface layer diffraction and refraction, diffusion of photogenerated carriers in the semiconductor bulk, carrier transit to and in the inversion layer, image motion, finite cell size, and transfer inefficiency in the readout process.

The surface layers affect quantum efficiency via the transmissivity and absorption in the layers of the surface structure. The surface layers affect the MTF by near field diffraction of light by the gate lines and for non-zero incident light angles by multiple reflections in the surface thin film layers (210).

If photons are absorbed within the depletion regions, then the collection process is 100 percent efficient. However, if photons are absorbed away from the depletion regions, then the charge configuration will spread as it diffuses toward the depletion regions, with a resulting decrease in MTF (91).

The imaging cell size affects the sensitivity profile of the potential well. This effect is defined as the integration MTF which is given by the Fourier transform of the basic integration cell. For a rectangular cell of length Δx repeated with periodicity P , the integration MTF is

$$\text{MTF}_{\text{integ}} = \frac{\sin \frac{f}{f_{\text{max}}} \frac{\pi \Delta x}{P}}{\frac{f}{f_{\text{max}}} \frac{\pi \Delta x}{P}} \quad (4.25)$$

where f/f_{max} is the spatial frequency of the image. For 2:1 interlace, $f_{\text{max}} = 1/P$. For $\Delta x = P$, the first zero in the MTF occurs at $f = f_{\text{max}} = 1/P$. For $\Delta x = P/2$, the first zero occurs at $f_{\text{max}} = 2/P$. Figure 4.56 shows the integration MTF versus normalized spatial frequency for $\Delta x = P/2$ and $\Delta x = P$.

The effects of transfer inefficiency on MTF are identical to the transfer inefficiency effects in CCD analog delay circuits and will be defined as transfer MTF. During the transfer of a sampled sinusoid along a CCD shift register, a fraction of the charge ϵ is lost from each of the samples at each transfer, and this charge is added to trailing samples. The effect of this dispersion on MTF is given by

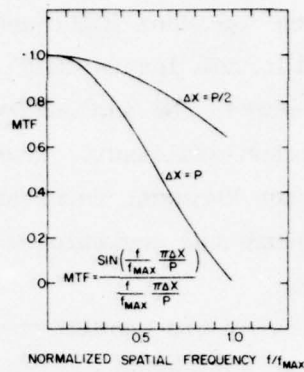
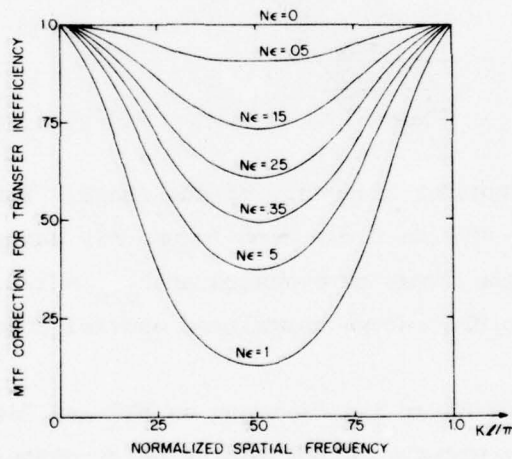


Figure 4.56. Integration MTF versus normalized spatial frequency (after 91).



MTF Correction for Transfer Inefficiency for a Two-Field Readout

Figure 4.57. Transfer MTF versus normalized spatial frequency (after 146).

$$MTF_{\text{transfer}} = \exp \left\{ -n \epsilon \left[1 - \cos \left(\frac{\pi f}{f_{\text{max}}} \right) \right] \right\} \quad (4.26)$$

Figure 4.57 shows the transfer MTF versus normalized spatial frequency. The symmetry of the curves can be easily explained. The Nyquist frequency is $1/P$ for a 2:1 interlaced array. Also, the sampling in any field occurs at spatial frequency $1/P$. If the signal to be sampled is at spatial frequency f , then the frequency in the field is $f \leq 2/P$. However, if $1/P \leq f \leq 2/P$, the frequency in the field is $1/P - f$, which results in the symmetrical curves.

The calculated vertical and horizontal MTF characteristics for the previously described 190×244 element array with transfer inefficiency and a parameter are shown in Figure 4.58.

4.3.3.2. Blooming. Image blooming in an imager is a detrimental characteristic and precautions are usually taken in the design of the imager to minimize blooming effects. Blooming is characterized as an apparent increase in the size of an image of a bright object under overload conditions and in some cases it can wash out most of the picture information. In a CCD blooming condition, excess carriers from a localized overload can diffuse through the bulk to neighboring potential wells. In addition, the charge can spread preferentially along the transfer channels, producing white streaks in the display as shown in Figure 4.59. The streaking phenomenon is even more objectionable than circular blooming.

The only adequate method known for complete blooming suppression is a charge overflow sink, which for complete blooming suppression must be applied to every sensor element. The device complexity is therefore considerably increased (75).

The organization of a CCD frame-transfer device with overflow sinks, for blooming suppression is shown in Figure 4.60. These overflow sinks drain off excess charge that might otherwise spill into neighboring potential wells.

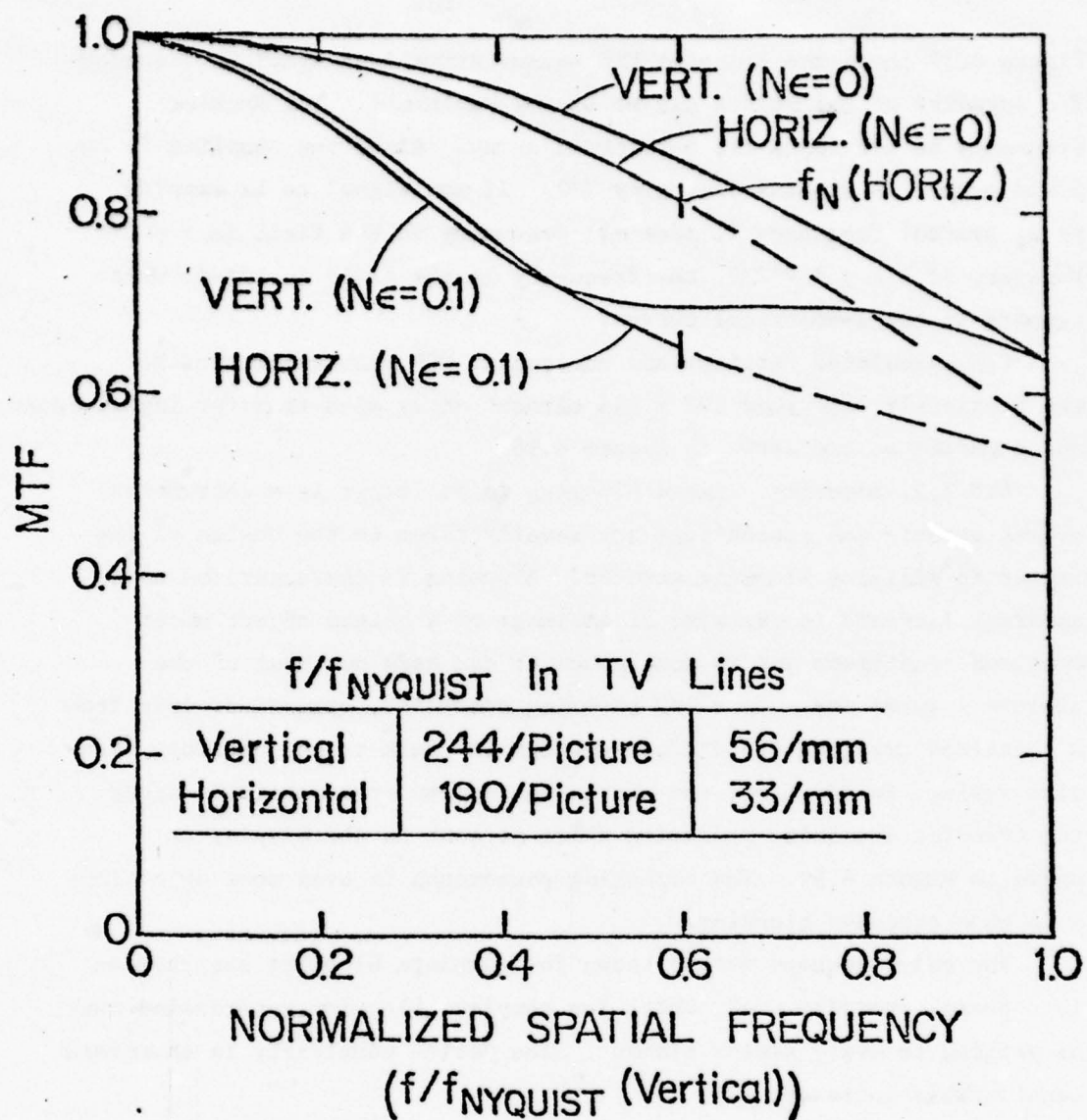


Figure 4.58. Calculated MTF characteristics of the 190 x 244 element imaging array (after 75).



Figure 4.59. Channel blooming in a charge-coupled imaging device with frame transfer organization. (a) Caused by reflections on glasses (b) Caused by the radiation from a match and a cigarette (after 147).

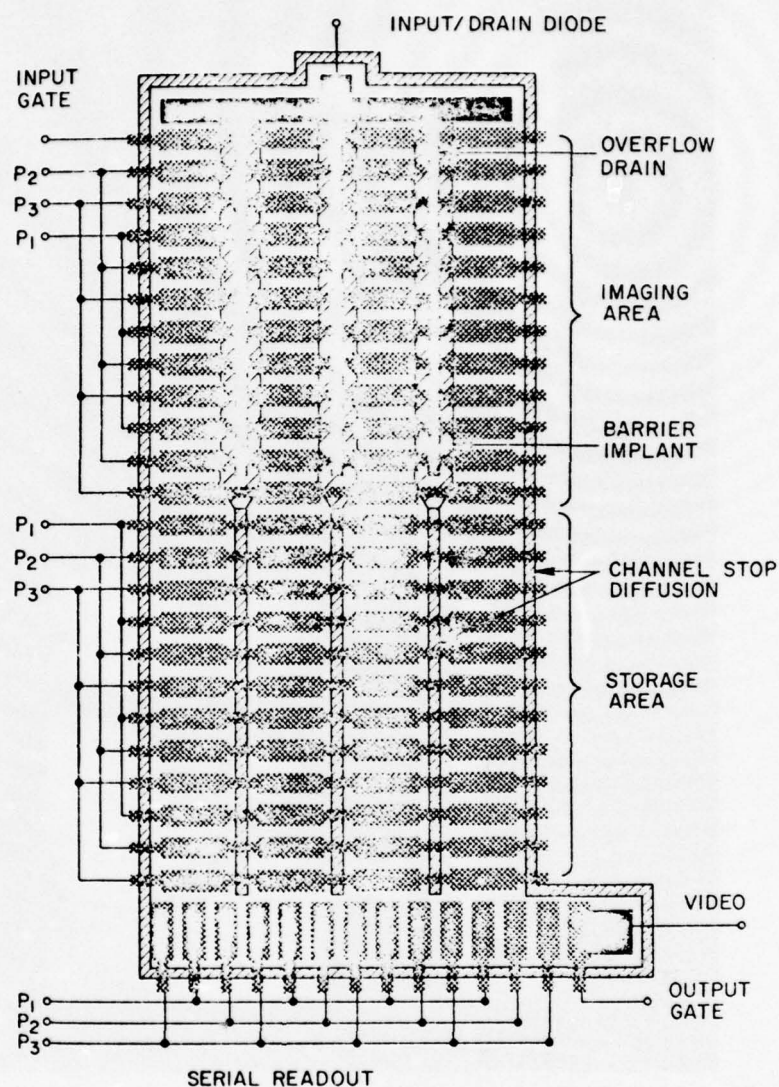


Figure 4.60. Organization of a CCD area image sensor with frame-transfer organization and overflow sinks placed between the vertical transfer channels for blooming suppression (after 159).

CID structures are inherently resistant to blooming since each sensing site is electrically isolated from its neighbors. Charge spreading in the substrate is minimized by the underlying charge collector (207). Figure 4.55 was produced by a 244 x 248 element CID imager exposed to a high contrast scene. The camera utilized a modified parallel injection readout method that is highly resistant to image blooming, as indicated by the automobile headlamps. The blooming suppression in the parallel injection CID approach occurs because the half-select and injection operations occur during the horizontal blanking interval. While excess charge can accumulate during a line scan interval and cause column brightening for overloads occurring in the right-hand portion of the image field, this effect is attenuated by the line-to-line frame integration time ratio.

4.3.3.3. Quantum efficiency and spectral responsivity. The responsivity of a solid-state imager depends on the electrooptical properties of the semiconductor. CCD image sensors can have quantum efficiencies close to the theoretical limit when backside illuminated. However, when frontside illumination is used, the complicated electrode structure can result in the loss of a large portion of the incident light by reflection and absorption. For opaque electrodes separated by gaps, the reduction in sensitivity is simply the ratio of the opaque electrode area to the total cell area. In the case of semi-transparent electrodes, such as polysilicon, loss results from absorption and from the reflections at the various silicon-silicon dioxide interfaces, which cause wavelength dependent interferences. Therefore the spectral transmission curve and the response of the device shows peaks and valleys (see Fig. 5.44). On the average, a response loss of a factor of two to three is incurred when light is transmitted through a polysilicon electrode structure, with a large loss in the blue region. Average values for the quantum efficiency of sensors fabricated so far range around 25% with absolute responsivity of

0.1 to 0.2 A/W (9).

A CID electrode using metal oxides (211, 212) has increased the sensitivity and flattened and extended the spectral response to the blue range. Figure 4.61 shows the quantum efficiency and spectral response characteristic of one of these devices, which has a nearly uniform spectral response from 400 to 800 nm and a 70% quantum efficiency. Figure 4.62 shows the transmittance of an indium-tin oxide film compared to that of a polysilicon film. The absorption in the polysilicon film at reduced wavelengths is apparent.

4.3.3.4. Low light level imaging. In low light level imager applications, signal-to-noise ratio and resolution are related. As the signal-to-noise ratio falls below a certain value, the response from an individual resolution element starts to lose its significance and the signals require averaging over several elements in order to extract meaningful information. Studies (213) have indicated that the signal-to-noise ratio for the charge packets originating from a fixed location in a solid-state image sensor in the presence of a static input pattern must exceed a value of five in order not to impair the maximum resolution determined by the geometry of the device.

The irradiance H required to obtain a signal-to-noise ratio, K , in an area occupied by one sensor element of area W^2 is (213)

$$H = \frac{K\bar{N}}{C\theta t W^2} \frac{L_{OBS}}{L_{GEOM}} \quad (4.27)$$

where \bar{N} is the average noise per packet, C is the contrast of the scene, θ is the sensor quantum efficiency, t is the integration time, W is the linear dimension of the assumed square sensor cell, L_{OBS} is the total number of observable TV lines in the picture height and L_{GEOM} is the maximum possible number of TV lines in the picture height dictated by the cell geometry. C (contrast) is defined as $\frac{\Delta N_s}{N_s}$ where ΔN_s is the modulation of the signal N_s . This equation indicates that in

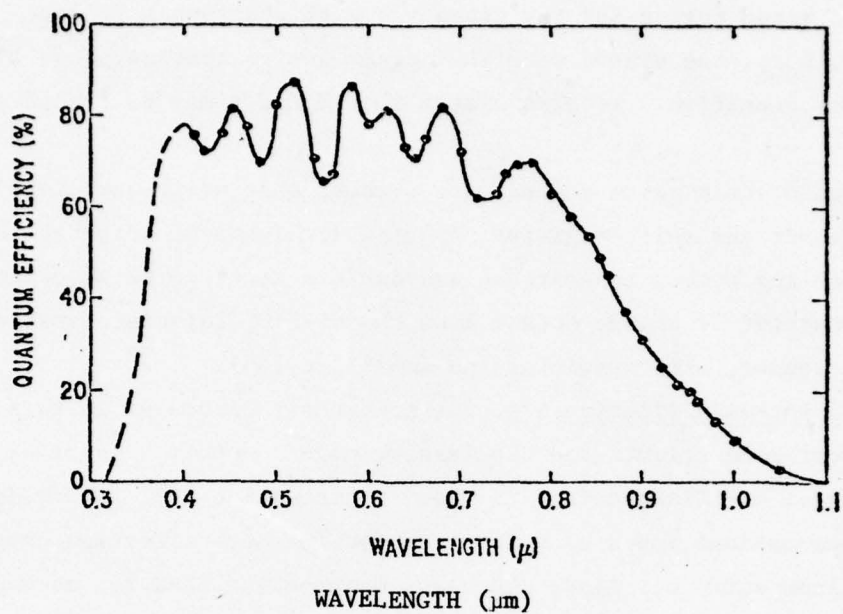


Figure 4.61. Quantum efficiency and spectral response of a metal oxide electrode CID imager.

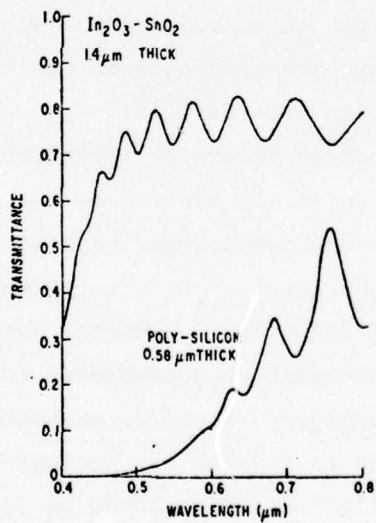


Figure 4.62. Transmittance spectra in the visible region of indium-tin oxide compared to that of polysilicon (after 212).

the noise-limited region for any given value of observable TV line resolution, L_{OBS} , the sensor with the larger active imaging area, W^2 , will be more sensitive. It also states that H and t may be traded off directly.

The sensor chip noise sources are thermal shot noise associated with the sensor and shift register, Nyquist (or Johnson) noise at the reset switch and output capacitance and surface state noise associated with the transfer of charge to and from the $Si-SiO_2$ interface states within the sensor, shift register and amplifier (66).

4.3.4. Backside Illumination. As previously discussed in this report, front-side illuminated CCD imagers have a number of optical disadvantages: one disadvantage is that the frontside SiO_2 layers do not have the optimum index of refraction for the antireflection coating of the silicon surface. Also, the glass overcoating used for mechanical chip protection causes an additional deviation from the optimum total antireflection coating thickness. Any opaque electrodes reduce the effective imaging area. Polysilicon electrode absorption of blue light and interferences at the interfaces of the multilayer structure cause fluctuations in the spectral response of the imager which is of particular importance in color cameras (214).

The problems encountered in frontside illuminated CCD imagers can be eliminated when the device is illuminated on the back side. However, with backside illumination, the device must be thinned to less than the sensor element center-to-center spacing to prevent significant lateral diffusion of the photogenerated minority carriers. After thinning, the silicon surface must be accumulated to minimize carrier recombination at the back surface. Finally, an antireflection coating is deposited on the backside to improve the optical transmission.

The devices are normally thinned to 20-30 μm (214,215). A 4 phase anodized aluminum electrode structure imager was thinned to less than 30 μm with less than 1 μm variation. Usually the rim of the

device is not thinned as much as the center imaging portion to provide mechanical support for the imaging portion and to allow lead bonding to the chip without breakage. However, this selective thinning is very difficult to accomplish reproducibly and the trend today is away from backside illumination.

Figure 4.63 shows responsivity characteristics of a thinned four-phase linear 500 element backside illuminated CCD imager and a frontside illuminated three-phase 100x150 element area imager. The smoothness and amplitude of the backside illuminated device curve indicates the improvement which can be obtained with backside illumination. The curve peaks at about 700 nm with a quantum efficiency of about 90% and exceeds 50% for a spectral range from 500 to 900 nm. The decrease in quantum efficiency at the longer wavelengths is due to the thinness of the silicon material and the long infrared absorption length. At the shorter wavelengths, the decrease in quantum efficiency is due to both backside surface recombination and bulk recombination (214).

It should be noted that backside-illumination cannot be used with the interline transfer organization since the vertical transfer channels cannot be easily shielded to prevent carriers from diffusing directly into the storage registers.

4.3.5. Infrared Image Sensors. CCD infrared image sensors are a relatively new area of application for CCD's and a significant amount of work is now being done in this area (216, 217). The types of infrared CCD's (IRCCD's) which have been explored fall into two categories of devices - monolithic and hybrid (216).

The monolithic IRCCD's usually use a conventional CCD structure on a narrow bandgap or extrinsic semiconductor sensitive to IR radiation, or combine a Schottky-barrier internal sensing array with a CCD readout technique.

The hybrid versions consist of one of several possible types of

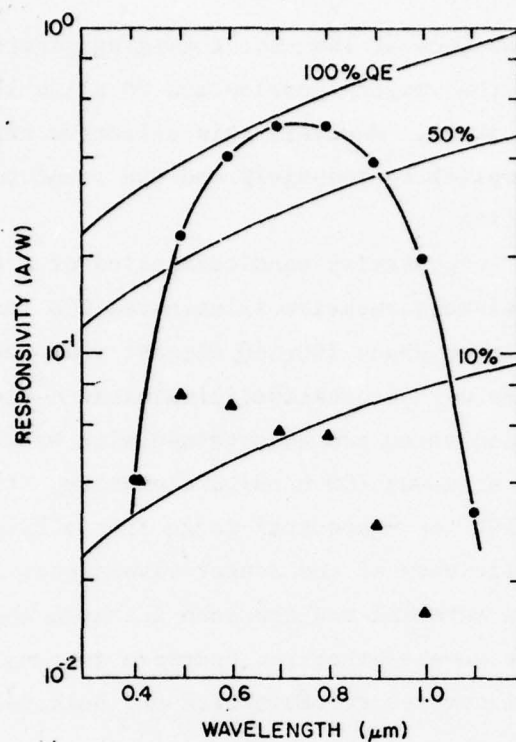


Figure 4.63. Spectral responsivity of: ●, thinned four-phase linear 500-element backside-illuminated CCD imager, and ▲, frontside-illuminated three-phase 100 x 150 element area imager (after 214).

IR detectors connected to a conventional CCD shift register. The purpose of the silicon CCD in this case is to perform signal processing functions such as multiplexing, amplification, correlation, delay, scanning, etc. Hybrid IRCCD's can be subdivided into two classes -- direct and indirect injection devices. In the direct injection device, photogenerated charge is injected directly from the IR detector into the CCD whereas the indirect injection device adds a buffer between the IR detector and the CCD circuit (216).

IR applications cover many fields including military, industrial, medical and scientific with the military interest being the largest.

IR devices generally operate in one of three of the atmospheric transmission windows present at 2.0-2.5 μm , 3.5-4.2 μm , and 8-14 μm . An important point to consider in IR imaging applications is that the contrast ratio between the photon flux generated by an incremental change in background temperature and the total photon flux is typically in the range of 1.0 percent in the 2.0-2.5 μm window and less than 0.1 percent in the 8-14 μm window both for 0.1°K change (typical for IR imaging) in the 300°K background. These low contrast ratios require extremely good uniformity in the IR materials. In addition, most IR detectors operate at reduced temperatures and a cooling system is required.

4.3.5.1. Monolithic IRCCD's. Monolithic IRCCD's include both inversion-mode and accumulation-mode devices. The operation of the inversion mode device is essentially the same as silicon CCD devices except that the device is fabricated on a narrow bandgap semiconductor material. The bandgap of the semiconductor determines the absorption peak and therefore the IR window. The narrow bandgap semiconductors are the III-V, II-VI and IV-VI compounds and consist of materials such as InAs, InSb, $\text{Hg}_{1-x}\text{Cd}_x$, Te, PbTe and $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$ (216).

Accumulation-mode devices operate by inducing the same majority carrier type at the insulator-semiconductor interface as in the bulk

of the semiconductor. In this way, an extrinsic substrate can be used. The IR absorption peak is determined by the ionization energy of the impurity levels. The peak response of gold-doped germanium occurs at $8\text{ }\mu\text{m}$ and Ga-doped Si at $17\text{ }\mu\text{m}$. The devices operate in a similar manner to conventional CCD devices. One accumulation-mode device (206) uses a two-layer overlapping gate structure. This 64-cell n-channel device was built on a phosphorous-doped Si substrate and demonstrated a transfer efficiency of 0.99 per gate at 25 KHz at 4.2°K .

Schottky-barrier IRCCD's can be made based on the internal photo-emission from metal-semiconductor arrays on silicon. Photons of energy are absorbed in the metal resulting in the excitation of a hot carrier which is emitted into the semiconductor. The emitted current is integrated by a negative charge accumulation method.

Monolithic CCD devices have also been used for IR sensing using InSb (218).

4.3.5.2, Hybrid IRCCD's. Hybrid IRCCD's have received more attention to date than monolithic versions due to the fact that fewer device compromises are incurred if the IR sensor and signal processing circuits are separated.

As previously stated, in the direct injection IRCCD, the photo-generated charge is directly injected into the CCD shift register thus implying a DC coupled system. Thus, only detectors with very small DC currents such as photovoltaic and extrinsic detectors can be used in order to prevent overloading the CCD.

The basic direct injection concept is illustrated in Figure 4.64 for an N-on-P IR photodiode and an n-channel CCD. The IR diode is connected to a silicon coupling diode on the CCD chip. The MOS input gate of the CCD reverse biases the IR diode and the transfer (XFER) gate introduces the photodiode current into the CCD.

Indirect injection IRCCD's use a buffer stage between the photo-detection stage and the CCD shift register. Two types of indirect

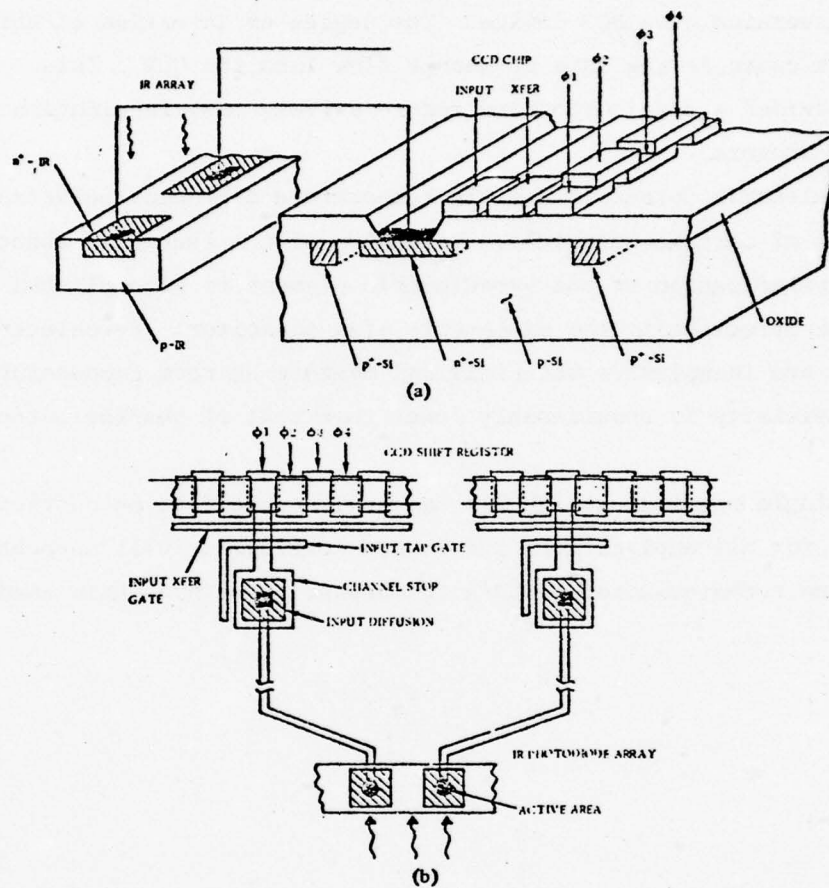


Figure 4.64. Direct injection hybrid IRCCD a) coupling concept, b) array layout (after 216).

injection devices are pyroelectric detectors and photoconductive thin films.

In the photoconductive film technique, a photoconductive film is deposited on silicon dioxide and is used to directly influence the channel inversion of a MOS device. The degree of inversion of this transistor controls the rate of charge flow into the CCD. This scheme provided a straightforward and relatively easy fabrication method for IRCCD imagers.

Pyroelectric detectors use the temperature dependent polarization properties of certain materials. Detection of the thermally induced electric polarization of the pyroelectric element is accomplished by making the pyroelectric the dielectric of a capacitor. Pyroelectric detectors use inexpensive materials and operate at room temperature but their sensitivity is considerably lower than that of quantum detectors (216).

No single approach to IRCCD's has proven itself to be sufficiently versatile for all applications and future development will undoubtedly present new techniques for IRCCD's to surpass those presently used.

5. DISCUSSION AND SUMMARY

5.1. Processing Status and Problem Areas

Currently, there are several processes used in the development and small-scale production applications of CCD's, but 2 of these are most widely employed in industry due to economic, performance, and reliability considerations. Because of reliability and tolerance criteria overlapping electrodes are required. For circuits with clock frequencies less than 5 MHz, the simple p-channel process with one level of polysilicon and one level of aluminum metalization is the main contender with the anodized double aluminum metalization system also in the running. For higher performance circuit applications, the surface and bulk n-channel process using two levels of p-doped polysilicon and one aluminum metalization layer is the primary process being used in the industry. For very high frequency circuit performance (~ 100 MHz), the profiled bulk channel process is presently the only possibility, but this process is still in the development stage.

Since CCD circuits went from the small trivial circuits to very large complex circuits without really passing through the medium-scale integrated circuit region, one of the most significant problems facing the industry is the problem of processing defects and the resulting low yield. In many large imager applications (250×250 to 500×500), the physical dimensions of the chip are greater than $1 \text{ cm} \times 1 \text{ cm}$ and thus random defects which could be ignored for smaller chip sizes become extremely important. In order to get perfect masks, iron oxide and non-reflecting chrome masks are being used extensively, and projection mask alignment is becoming more popular after the solution of some significant problems. Etching tolerances of oxide, polysilicon and metal layers are decreasing with $5.0 \text{ } \mu\text{m}$ lines and $5.0 \text{ } \mu\text{m}$ spacings being generally accepted as the current minimum dimensions. Techniques such as wafer scrubbing, plasma etching, all-ion-implanted structure

(except for polysilicon doping), decreasing furnace temperatures ($<1100^{\circ}\text{C}$), etc. are all being considered and used to some extent to minimize the defect problem. Fortunately, one of the major problem areas of integrated circuits, namely contact window etching, is greatly reduced for CCD devices since large portions of CCD circuits are contactless structures. One problem which ordinary integrated circuits do not have which strongly affects CCD performance is dark current generation. The main source of dark current is currently considered to be due to initial wafer and process-induced lattice defects. Float-zone crystal growth is considered to be currently the best growth method from the standpoint of wafer lattice defects. To decrease process-induced lattice defects, lower furnace temperatures, improved preheating and cooling techniques, oxidation and anneal cycles using ambients such as 2% HCl, etc. are currently being used. Also, to induce a diffusion of impurities and lattice defects from the front side to the backside of the wafer, defects are induced on the backside of the wafer to attract dark current generating damage sites and impurities away from the frontside. Heavy phosphorus diffusions and implants, argon implants, grinding or sandblasting, etc. are some of the backside wafer techniques currently being investigated to decrease the dark current via decreasing the damage induced generation site on the front surface of the wafer.

5.2. Circuit Status and Problem Areas

The level of integration of CCD circuits has progressed to the point of where the CCD state-of-the-art readily allows 50 to 100 thousand MOS gates to be fabricated on a chip of 200 to 250 mils per side and even larger levels of integration are being developed.

16,384 bit quasi-serial CCD digital memories are available from Fairchild Semiconductor (CCD 460) and Intel (2416). The Fairchild device was described in the Digital Circuits section of this report. A 65,536 bit CCD digital serial memory is reportedly available from Mnemonics, Inc.

Analog CCD devices do not lend themselves to standardization as readily as digital devices and for this reason very few analog CCD devices are available as standard commercial devices. One analog device which is available is the Fairchild CCD 311, a 260-bit analog shift register. However, analog CCD devices are available on a custom design basis from several manufacturers.

Linear image sensor arrays are also available from several manufacturers. Among these is the Fairchild CCD 121, a 1728 element linear image sensor.

Area image sensors with approximately half of conventional TV resolution are also available and several of these have been described in this report. Among these are the Fairchild AID244, a 190 x 244 element CCD Area Imaging Device and the General Electric 244 x 248 element CID area imaging array.

New CCD devices will continue to be introduced at an increasing rate and many of these new devices will contain more elements than presently available devices, with increased device density and improved performance.

The buried channel CCD device will probably become the CCD technology standard, replacing surface channel technology. N-channel technology will also become the process standard because of its higher frequency response.

The major problem areas in CCD circuits are low yield and high dark currents (leakage). The low yield is due to the fact that the level of integration attempted with CCD circuits is progressing as fast or faster than the process technology. However, the semiconductor industry has always operated in this manner. The dark current of the favored buried channel process is higher than the dark current of surface channel processes and many buried channel devices must be operated at low temperature to reduce the dark current and obtain acceptable performance. However, the dark current problems will undoubtedly be

CCD CHIPS

Ref. No.	Bits/Chip	Worst Case Access @ f (us @ MHz)	On-chip Power @ 1 MHz (uW/bit)	Chip Size (mils)	Area/Bit Chip/Cell (mils)	Chip Utilization	Technology
219	64r x 256b	128 @ 2	9	143x237	2.1/1.1	0.53	4 μ 2 level polysilicon gates
154	4x32rx128b (LARAM)	26 @ 5	10	220x200	2.7/1.5	0.57	1 μ 2 level polysilicon gates buried channel
220	9r x 1024b	512 @ 2	15	135x200	2.9/1.3	0.44	2 μ 2 level polysilicon gates buried channel
221	4x4k SPS	400 @ 10	1.5	136x169	1.4/0.57	0.40	2 μ 2 level polysilicon gates E/B operation
222	4x4k SPS	400 @ 10	10	124x350 (89x246)	2.7/1.2 (1.35/0.7)	0.45 (0.52)	3 μ 3 level 9 um polysilicon gates (same, with 7 um gates) ^a
223	16x4k SPS	400 @ 10	0.5	235x213	0.76/0.4	0.52	2 μ offset gate process

Figure 5.1. Chip sizes and bit areas of state-of-the-art CCD memory chips (after 218).

solved in the future as the technology progresses.

5.3. Yield and Area Considerations

Since CCD device technology is very similar to conventional dynamic MOS technology, used, for instance in the 4K bit dynamic MOS RAM's, it is expected that yield per unit area will be similar. Furthermore, the yield of a given device determines its economic viability, e.g. at any given time, there is a maximum chip size beyond which the costs per function increase so drastically that the device is not feasible. Under this assumption, the chip area per function is then the primary element of concern.

Figure 5.1 is a summary of data on a number of large CCD memory chips (218). The data in this table represent the state-of-the-art in CCD, which is constantly progressing. This table indicates the chip size, area per bit and technology of these state-of-the-art chips. It is seen from this table that the 2-level polysilicon gate process with electrode per bit (E/B) operation and the offset gate process result in the smallest bit area.

The major yield problem areas remaining are as follows:

- 1) Difficulty with polysilicon and aluminum etching due to 5 μm line widths and 5 μm line spacing.
- 2) Difficulty with deposited oxide and nitride pin holes creating interlevel shorts.
- 3) Contact holes in the peripheral circuit regions, e.g. shift registers and transfer devices.
- 4) Poor masks.
- 5) Contamination on wafers due to residual photoresist, dust, etc.
- 6) High dark current.
- 7) Threshold voltage uniformity.

5.4. Cost Considerations

The processing cost of both n-channel and p-channel CCD devices

is somewhat more expensive than conventional MOS processing because an additional gate electrode level is required, dark current control techniques are required, both gate threshold and field threshold control are required, additional ion implants for channel definition, barriers and buried channels may be required, and the initial wafer specifications on resistivity and dislocation density are more stringent than those for conventional MOS processes. However, notwithstanding these additional costs, the primary impetus in CCD technology is low cost per bit (or image element).

Manufacturers of CCD devices expect to maintain reasonable yields even as the device densities increase to an unprecedented level (224). The CCD device's increased functional density is due to two factors. First, it requires a smaller area for each bit. The 64,000 bit CCD memory recently described (223) has a per bit area of 0.8 mil^2 . Second, the number of contacts and diffusions is smaller, thus decreasing the effect of these yield-reducing steps and providing acceptable yield on larger chips than are practical with conventional MOS.

In 1975, the cost of CCD shift registers and MOS random access memories was comparable. However, in 1978 the price per bit spread is projected to be much greater, as shown in Figure 5.2. The reasons for this are twofold. First, the production process for CCD's was new in 1975. This tended to dictate lower yields and more conservative designs. In 1978 the process will be well defined and good yields can be expected. Second, the market for CCD's in 1975 was new and not as well defined or established as that of the read/write memories. In 1978 this situation will change drastically (225).

These predictions all assume conventional photolithographic processing, which is the factor that limits the minimum cell size. However, CCD bit sizes even smaller than 0.5 mil^2 are capable of operating without signal-to-noise ratios being degraded beyond the point of practical operation. Consequently, the exploitation of high-resolution

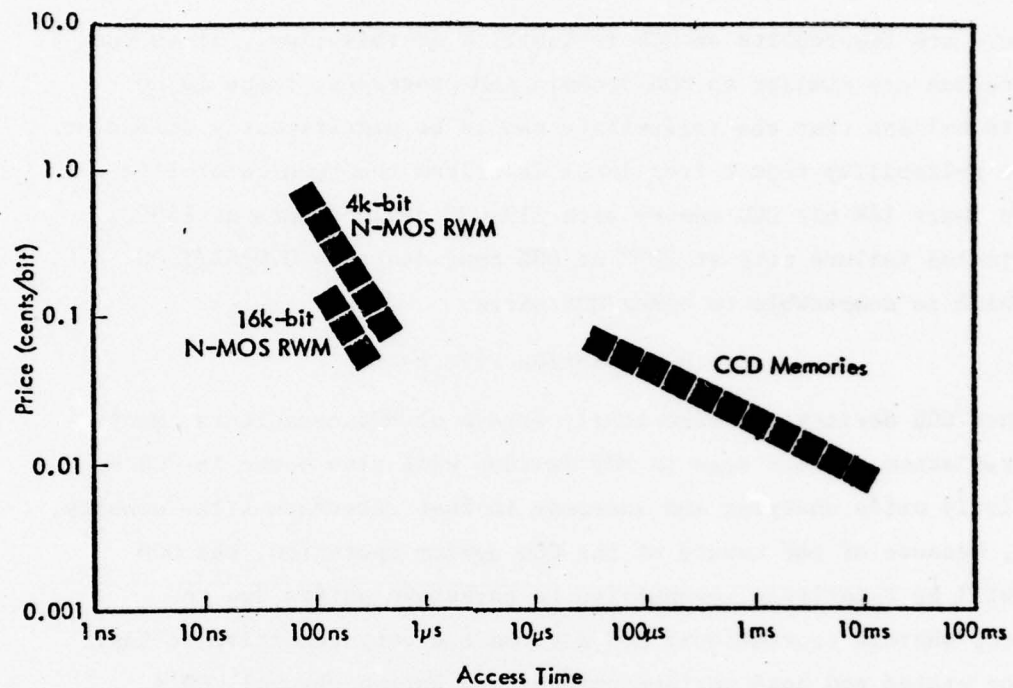


Figure 5.2. 1978 projected price/bit for CCD memories and read-write memories (RWM or RAM) (after 225).

electron-beam image definition in CCD fabrication appears likely.

5.5. Reliability

There are few reports on CCD reliability at this time. Since the CCD processes are similar to MOS dynamic RAM processes, there is no reason to believe that the reliability should be significantly different.

One reliability report from Intel describes the results of life tests on their 16K bit CCD memory with 119,000 device-hours at 160°C. The projected failure rate at 70°C at 60% confidence is 0.026%/1000 hours which is comparable to other MOS parts.

5.6 Radiation Effects

Since CCD devices are essentially arrays of MOS capacitors, many of the radiation effects seen in MOS devices will also occur in CCD's, particularly oxide charging and increase in fast interface state density. However, because of the nature of the CCD device operation, the CCD device will be relatively insensitive to threshold shifts due to radiation, whereas conventional MOS devices are very sensitive to fast interface states and both surface channel and buried channel CCD's are sensitive to dark current.

One device which has been characterized in a radiation environment is a 500-element three-phase surface channel shift register with planar aluminum electrodes (91). The radiation source was cobalt 60 gamma radiation. The flat-band voltage shift versus dose is shown in Figure 5.3 and the flat-band voltage increases almost directly with the logarithm of the dose. The transfer inefficiency radiation characteristic is shown in Figure 5.4. Approximately an order of magnitude increase in transfer inefficiency was observed at 3×10^4 rad. The increased transfer inefficiency is attributed to increased interface trapping. The fast interface state density and the dark current density are shown in Figure 5.5. Again, note the order of magnitude increase in interface state density and dark current at 3×10^4 rad.

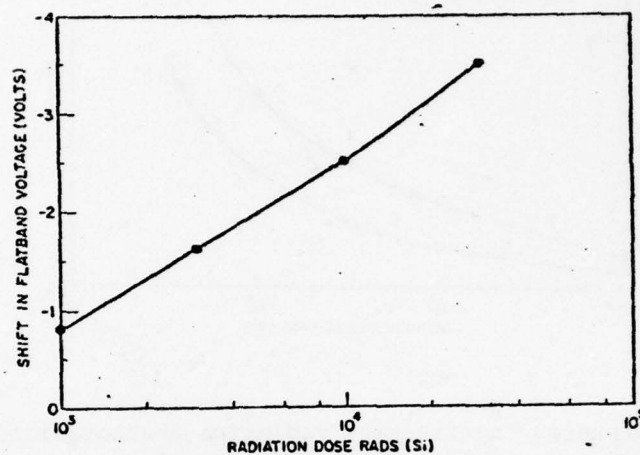


Figure 5.3. Shift in flat-band voltage versus radiation dose for 500 stage shift register (after 91).

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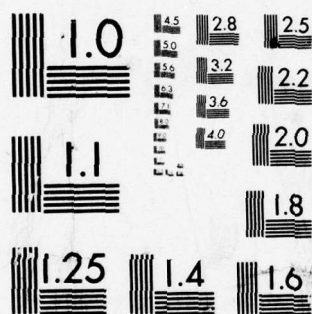


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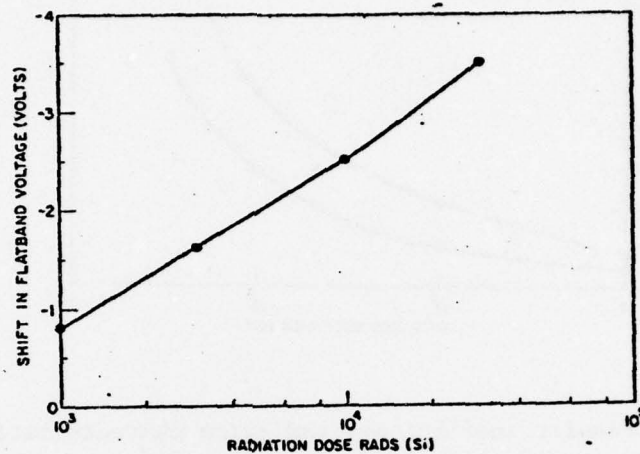


Figure 5.3. Shift in flat-band voltage versus radiation dose for 500 stage shift register (after 91).

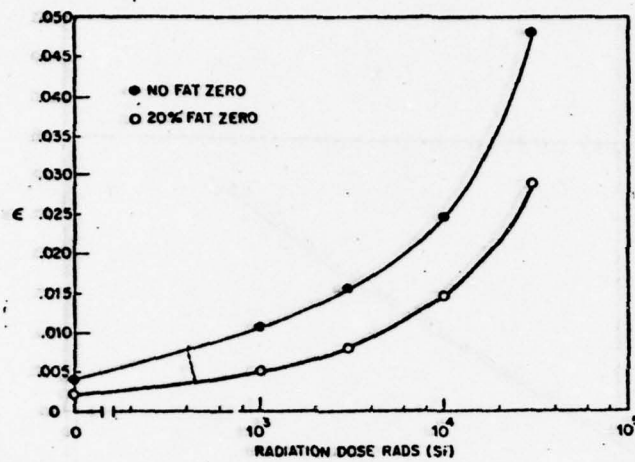


Figure 5.4. Transfer inefficiency radiation characteristic for 500 stage shift register (after 91).

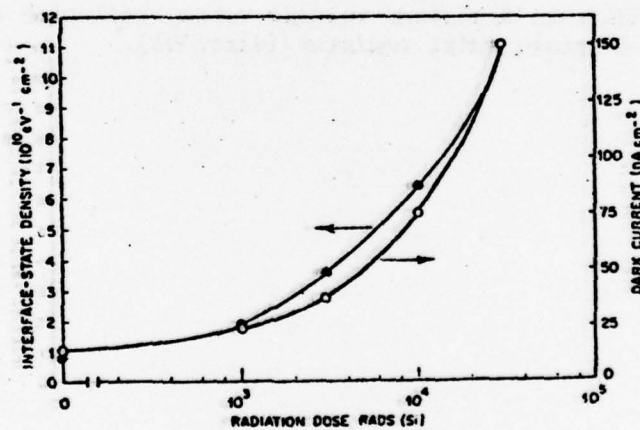


Figure 5.5. Interface state density and dark current radiation characteristics for 500 stage shift register (after 91).

A 64-element surface channel stepped oxide structure shift register with polysilicon and aluminum electrodes was also characterized under radiation (91). Figure 5.6 shows the flat-band voltage radiation characteristic, with a negative shift in flatband voltage occurring on both the aluminum and polysilicon electrodes. The transfer inefficiency curve is shown in Figure 5.7. Here, the preirradiation transfer inefficiency was recovered when the operating voltages were adjusted to compensate for the flatband shifts and re-establish the initial fat-zero level. However, at 3×10^5 rad, the formation of interface states resulted in an increase in the transfer inefficiency and also an increase in dark current occurred which could not be compensated by adjusting the operating voltages.

A 64-stage two-phase n-channel, buried channel, polysilicon and aluminum gate circuit was also tested under radiation (226). In this case, the radiation source was 1 MEV electrons. Figure 5.8 shows the channel turn-on voltage versus radiation dose. This characteristic is similar to that observed on the 64-element surface channel device just described, and can be compensated by adjusting the operating voltages. Figure 5.9 shows the transfer inefficiency characteristic of this device and it is seen that no significant degradation of transfer inefficiency occurs up to 10^5 rads. Figure 5.10 shows the dark current characteristic. No serious increases are observed up to 3×10^5 rad.

If buried channel CCD devices are used, and if the operating voltages are automatically varied by monitoring the flat-band voltage of a test device on chip, it appears that CCD's can be as radiation hard as the adjacent MOS circuits and should maintain satisfactory performance to about 5×10^5 rad(Si). (226).

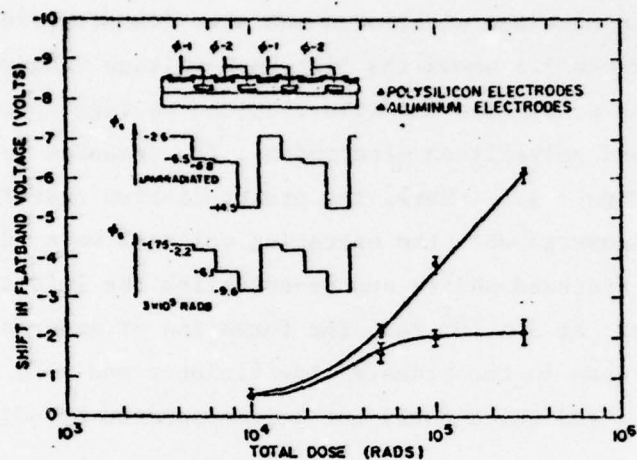


Figure 5.6. Shift in flat-band voltage versus radiation dose for 64-element shift register (after 91).

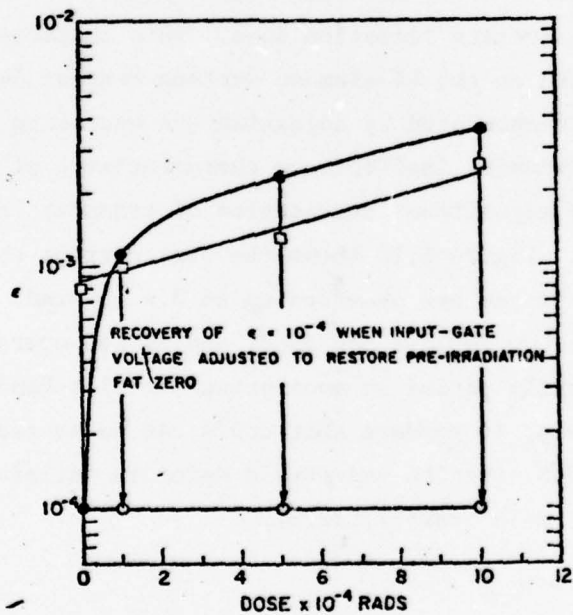


Figure 5.7. Transfer inefficiency characteristic for 64-element shift register (after 91).

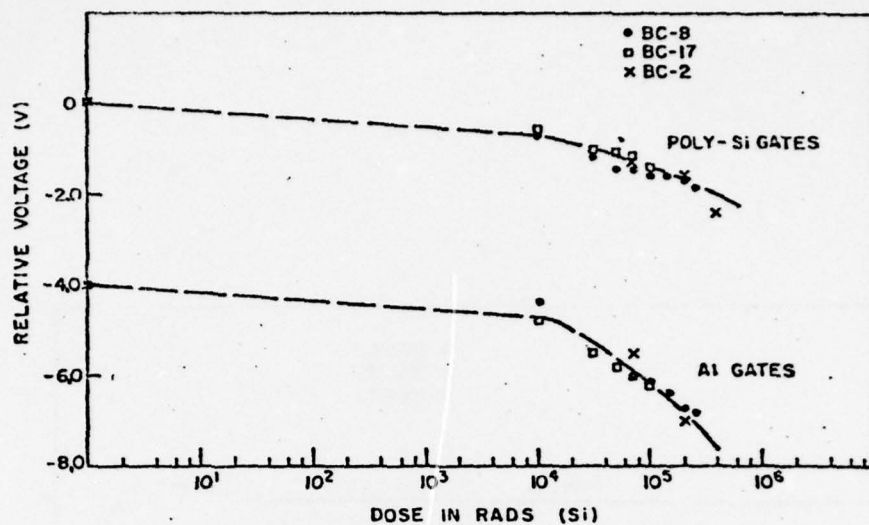


Figure 5.8. Channel turn-on voltage radiation characteristic for 64-stage buried channel device (after 226).

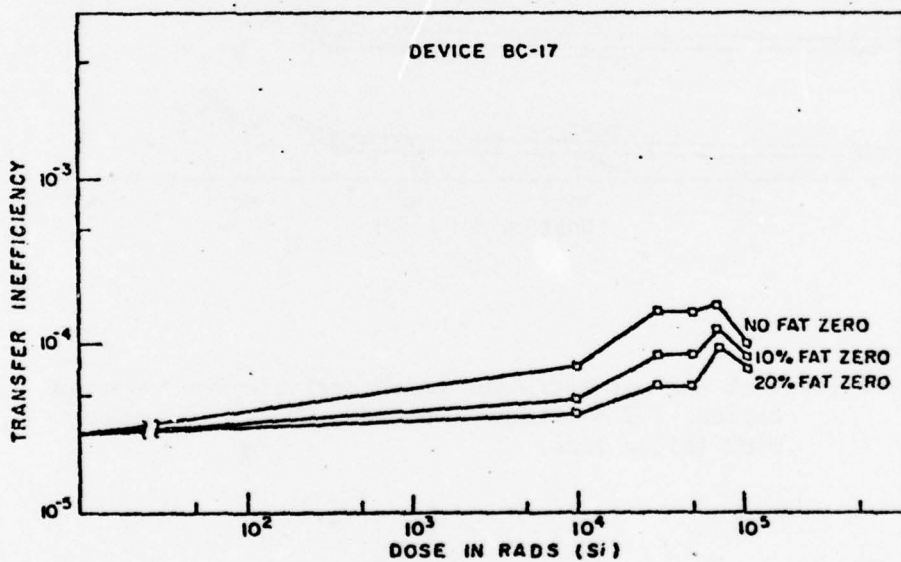


Figure 5.9. Transfer inefficiency radiation characteristic for 64-stage device (after 226).

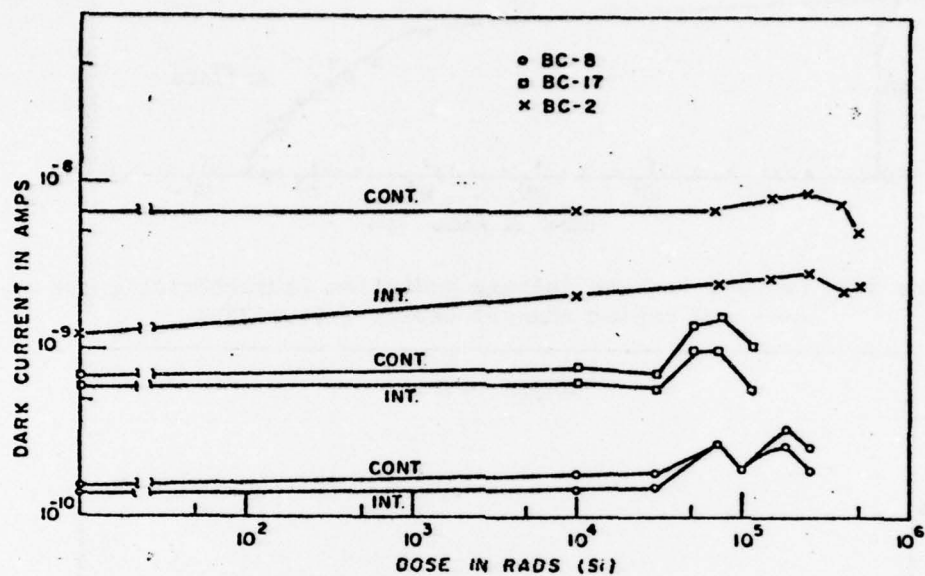


Figure 5.10. Dark current radiation characteristic for 64-stage device. INT = Integration mode, CONT = Continuous mode (after 226).

6. CONCLUSIONS, PROGNOSIS, AND RECOMMENDATIONS

6.1. Conclusions

The devices described in this paper rely on the basic concept of moving potential wells along a semiconductor surface. The CCD has progressed from the aluminum gap electrode device with its low yield and surface sensitivity to the modern overlapped gate polysilicon devices with their relatively good yield, reproducible characteristics and stability.

Even though a CCD can be considered as a special type of MOS device, the most useful description of the CCD is in terms of microscopic physical parameters rather than equivalent circuit models. To some degree, the same statement also applies to input and output circuits, especially where conventional MOS components join the CCD channels. This is due to the fact that conventional MOS circuits are described in terms of currents and voltages and their internal device transient time constants, such as the time to form and collapse an MOS channel, are much shorter than the circuit time constants. Thus conventional MOS devices can be considered as steady-state MOS channels that can be readily represented in equivalent circuit form.

However, the CCD transfer of small charge packets from one low capacitance CCD storage site to another involves very small transient currents. Therefore, the operation of CCD's is determined only by the transient channel characteristics rather than steady state. These transient channels are not amenable to equivalent circuit formulations.

It is interesting, however, that the theory developed for CCD operation has provided insight into new MOS components, such as the concept of charge pumping, the charge injection device, and the new 16K bit MOS RAM's. It is safe to conclude that the CCD principles developed to date will become accepted as integral parts of MOS circuit technology (227).

There are still aspects of CCD's where the current analysis technique of device operation are incomplete. This is especially true for CCD input and output circuits where linearity and noise are important.

A better understanding of interface states must be developed. Present techniques for characterizing the trapping process are subject to large uncertainties, although measurements of charge transfer inefficiency and transfer noise in surface channel CCD's can be used to characterize the effects of interface state densities on circuit performance.

A better understanding of the transfer behavior of very small charge packets needs to be developed. This is very important in determining the ultimate limit of detectability in low light level image sensors.

Since the basic CCD device operation is now fairly well understood, the present work is mostly being concentrated on fabricating large devices with practical functions, decreasing cost of processing, and increasing yield and reliability. Most devices now being fabricated use one to three levels of polysilicon and one layer of aluminum for bus lines and bonding pads. The use of polysilicon results in CCD devices with low interface state densities and good transfer efficiency. To a great extent, the real manufacturers of present CCD devices are using their standard silicon gate MOS process as a base process for CCD devices by adding a few steps to the basic MOS process to achieve the extra gate level(s), buried channels, etc.

Since the major impact of CCD devices will be in large arrays, particularly for memory and imaging, photolithography is now more important than ever. Optical mask exposure has reached its resolution limit and electron beam exposure seems to be the promising technique of the near future.

The source of dark current is very poorly understood at present and little is known about how dark current behaves under different

conditions. Reduction of high temperature processing, extreme cleanliness and gettering and annealing are all very important and can lead to devices with low dark current, although the physical phenomena involved are not well understood (9).

CCD memories are now emerging in large numbers. Several 16K bit chips are now available and a recently announced 64K bit chip (207) will be available in 1976. The storage capacity increase of CCD memories has been doubling annually, following the same curve as MOS RAM's, although the MOS RAM curve is decreasing in slope.

There are two major trends in CCD memory chip organization. One trend is for large, low cost, slow access systems, using serial-parallel-serial blocks with electrode per bit operation. The other trend is toward short access time, using short shift registers in a line addressed mode. The cost of these two approaches may differ by a factor of 2 and the access time may be different by a factor of 10. Multilevel storage with 2 bits per charge packet is a possibility for the future, although little work has been reported on it to date.

CCD memories require from $1/2$ to $1/4$ the area per bit than MOS RAM's. With the additional innovations of electrode per bit and multilevel storage, CCD's could have an order of magnitude cost advantage per bit over MOS RAM's in the future (218).

A simple calculation shows that if processing improves to 0.1 to 0.14 mil line-width capability, a CCD bit will require 0.1 to 0.2 square mils of silicon area. If the chip area is 50% utilized for storage and 2 bit per packet storage is used, a 200 x 200 mil chip will contain up to 4×10^5 bits. At a \$4.00 chip cost, the price per bit is one millicent. This is indeed impressive and would certainly result in widespread usage of CCD memories (218).

In addition to simple analog delay, an exciting function in analog CCD's is the transversal filter. Once a transversal filter is implemented, many other signal processing functions can be obtained.

These CCD's can be used to implement time-invariant finite impulse response (FIR) filters which can be constructed for pre-emphasis, de-emphasis or bandpass operation. Since the CCD clock frequency can be easily varied, so can the filter frequency response.

The quadrature filter implemented with CCD's is useful for providing single sideband modulation, and for providing the analytic signal representation of an arbitrary signal.

Tapped CCD's can be used to implement some important time varying filters. The discrete Fourier transform (DFT) can be implemented by means of fixed weight FIR filters and point-by-point multiplication. This implementation of the FFT is called the chirp-Z-transform (CZT) and allows direct computation of a DFT in real time.

There are several limitations in analog CCD's, primarily due to the fact that the analog signal is degraded as it is shifted through the array. Some of these limitations are caused by dark current, charge-transfer inefficiency, and clock noise. Other limitations result from the limited dynamic range, tap weight inaccuracy, and output signal amplifier nonlinearities. For an analog CCD to be really useful, signal-to-noise ratios greater than 40 dB and accuracy equal to 8-10 bits are required. In addition, the CCD frequency response is also important.

Electrically alterable filters will be required for future applications for matched filtering in signal detection and cross-correlation and convolution in adaptive filtering. Initial progress toward this goal has been obtained with the "charge sloshing" correlator. However, future systems will require correlation with analog or multilevel digital weights and this needs investigation.

For analog CCD's to really pay off in the future, high performance analog memories must be developed to store the analog signals during the signal processing.

To quote reference 228, "Perhaps the ultimate use of analog

signal processing with CCD's will take place in systems where the processing appears to be digital to the external user; but internally on the chip, the digital-to-analog and analog-to-digital conversions are performed using "charge" as the signal representation".

Since the CCD concept was introduced in 1970, solid state imaging technology has progressed tremendously. Area arrays have been operated which produce useful images down to light levels of 10^{-5} W/m^2 which correspond to starlight illumination on a medium reflectance, 100 percent contrast scene and produces 25 electrons per pixel in the highlights. The major issues in contention today in image array technology are surface channel versus buried channel, and frame transfer versus interline transfer versus CID. These issues will be discussed below.

The SCCD differs from the BCCD primarily in the location of the channel with respect to the semiconductor-insulator interface. The main advantage of the BCCD is that the channel does not interact with interface states. Therefore interface state trapping is not present and the need for a bias charge is eliminated. Charge packets in BCCD's do interact with bulk-trapping states; however, these trapping states are characterized by low densities and discrete energy levels. In practice, bulk trapping is not a problem for buried channel area arrays down to 10 electrons per pixel per frame. The BCCD also has a large fringing field component which aids charge transfer. This allows BCCD's to be operated with transfer inefficiencies of 10^{-4} or less up to 25 MHz.

The BCCD does require additional processing to implant the n-layer in the p-substrate and it has higher theoretical dark-current than the SCCD. The charge handling capacity of a shallow BCCD is about equivalent to that of a SCCD with 20 percent bias charge. Table 6.1 summarizes the characteristics of surface channel and buried channel area imaging arrays.

SURFACE CHANNEL/BURIED CHANNEL COMPARISONS

Surface Channel		Buried Channel
Limiting temporal noise	Surface trapping, hundreds of electrons	Bulk trapping, signal-level dependent, tens of electrons at low-signal levels
Limiting pattern "noise"	Nonuniform background charge Hundreds of electrons	Nonuniform dark current density, highly dependent on temperature, several electrons at -20°C
Detectivity limit	Hundreds of electrons	Tens of electrons, low-light level solid-state imaging possible
Speed limit ^a	< 10 MHz	25 MHz for shallow buried channels

^aAssuming standard photolithographic design rules.

Table 6.1. Surface channel/buried channel comparisons (after 229).

TRADEOFFS BETWEEN FRAME TRANSFER CCD, INTERLINE TRANSFER CCD AND CID AREA ARRAYS

	Frame Transfer CCD	Interline Transfer CCD	CID
Versatility	Frontside or backside illumination possible, can be used for TDI	Frontside illumination only, separate sensors make video signal processing possible	Frontside illumination only with epi-CID, different design required for backside illumination, random readout possible
Sensitivity	Large fraction of theoretical silicon response in backside illuminated mode	Less than theoretical silicon response by a factor between 2 and 4 due to frontside layers and shielded vertical registers	Large fraction of theoretical silicon response in backside illuminated mode
Anti-blooming control	Accumulation around cells can be used in surface channel arrays	Drain diodes between columns can be designed into the array to provide column anti-blooming	Accumulation around cells and the epi-substrate junction provide excellent anti-blooming control
Integration MTF at limiting resolution:			
Vertical ^a	0	0.6	0.6-0.9
Horizontal	0.6	0.9	0.6-0.9
Problems	High-speed vertical transfer	Complex cell	Pattern "noise"

^aWith 2:1 vertical interlacing.

Table 6.2. Tradeoffs between frame transfer CCD, interline transfer CCD and CID area arrays.

CCD's have been fabricated and evaluated in two different designs - frame transfer (FT) and interline transfer (IT). The CID is a third array design. Table 6.2 lists some of the important tradeoffs between FT, IT and CID arrays.

The FT organization allows front or backside illumination. The IT array can only be front side illuminated because the transport registers cannot be shielded from the backside. The CID array can be backside illuminated if a design modification is made. The CID array also allows random access to image sites which may be useful for tracking.

With frontside illumination, all three organizations suffer from a loss of sensitivity due to reflection at the frontside layer interfaces and absorption by the polysilicon electrodes. In addition, the IT organization suffers from the loss of photons which fall on the opaque regions which shield the vertical transport registers.

Antiblooming control can be designed into all 3 types of arrays. Useful antiblooming control up to about 10 times saturation can be achieved in FT and CID arrays by biasing the regions around the cells into accumulation during integration. Some degree of antiblooming control can be achieved with IT arrays with drain diodes between the vertical transport registers.

Other problems of the 3 array organizations are 1) the high-speed vertical transfer from the imaging section into the storage section in FT arrays, 2) the fabrication complexity of the IT cell, and 3) susceptibility of CID arrays to pattern "noise" associated with the X-Y readout technique (229).

6.2. Prognosis

CCD technology will find wide acceptance. The basic CCD device requires few junction diffusions and contacts and the functional packing density is extremely high.

The two major areas of application will be self-scanned image sensors and digital shift register memories.

CCD imaging devices will ultimately replace silicon vidicons (225). The use of silicon vidicon devices will correspondingly decline within the next 5 years.

At this time there is no clear winner in the competition between FT, IT and CID arrays. For the commercial market, the winner will probably be the one which produces TV quality images first and can produce the parts in quantity (229). For military applications, all 3 array types will probably co-exist for several years because each has characteristics valuable to such applications.

In CCD memories, the first parts will span the storage region from 16K to 64K bits per chip at shift rates from 2 to 5 MHz. CCD memories for digital computers are not merely replacements for RAM's or disks. They are a new cost effective component in the memory hierarchy having access times much faster than drums or disks but slower than core memory or MOS RAM's. They will find totally new markets as computer architecture is designed to utilize their unique characteristics.

By 1985 the CCD memory cost per bit will be on the order of 0.006 cents with an average access time of 6.4 μ seconds and 128K bits per chip.

6.3. Recommendations

CCD's are finding increasing applications and it appears that they will have a future in large systems. It appears premature, however, to incorporate CCD's into complex systems which are expected to have a long life and high reliability.

A) New parts are continually being introduced and standard products are difficult to identify at this time. This might make replacement difficult.

B) Little is known yet about reliability. Although in principle, CCD's should be comparable to MOS circuits in reliability, the effects of the different processing steps involved are not determined.

C) CCD technology is progressing rapidly but some of the physical processes influencing operation are not well understood. If, for example, the carrier generation rate could be reduced substantially, considerable improvement in performance could be achieved in memories, imagers etc., causing existing parts to become obsolete.

It is recommended that the FAA not include CCD's in complex systems at this time, but should follow their development along with that of other technologies. The use of CCD's should be reexamined in about 1978.

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